**OKI** Semiconductor

This version: Nov. 1997
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# MSM9000B-xx

**DOT MATRIX LCD CONTROLLER**

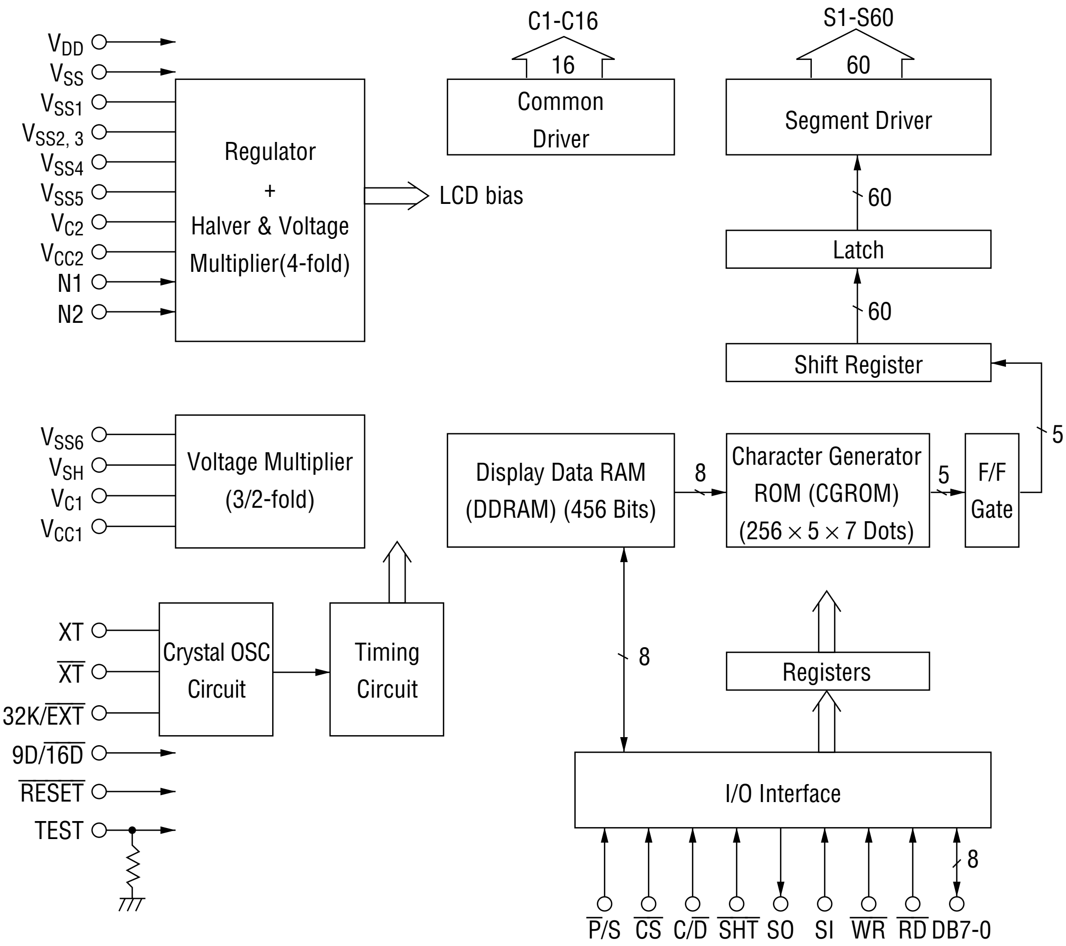
## GENERAL DESCRIPTION

The MSM9000B-xx is a dot-matrix LCD control driver which has functions of displaying 12 (5 x 7 dots) characters (2 lines) and 120-dot arbitrators.
The MSM9000B-xx is provided with a 16-dot common driver, 60-dot segment driver, Display Data RAM (DDRAM), and Character Generator ROM (CGROM).
This device can be controlled with commands entered through the serial interface or parallel interface.
The font data in the CGROM can be changed by mask option.
Since the MSM9000B-xx has an LCD driving bias generator circuit, LCD bias voltages can be obtained by merely providing a required capacitance externally.
The MSM9000B-xx is applicable to a variety of LCD panels by controlling the contrast.

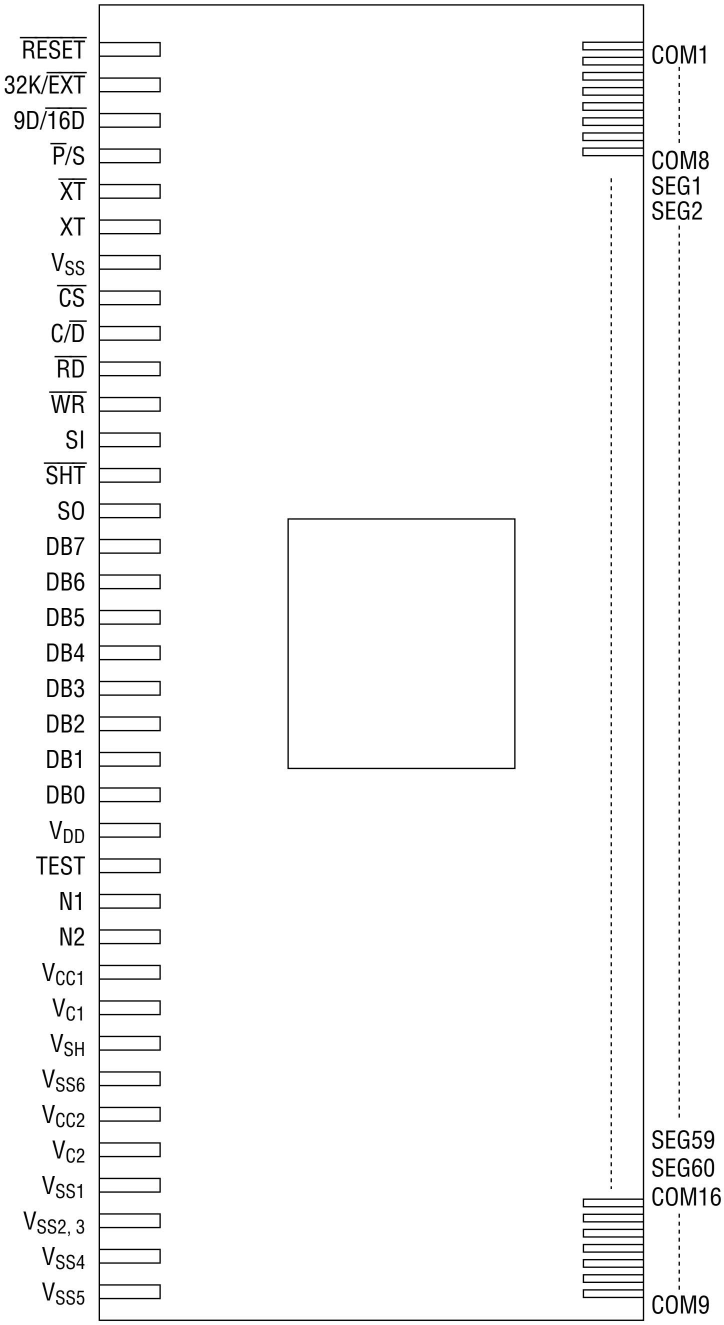
## FEATURES

- Logic voltage($V_{DD}$): 2.5 to 3.3 V
- LCD driving voltage($V_{BI}$) : 3.0 to 5.5 V
- Low current consumption: 35 μA max.(operating)
- Switchable between 8-bit serial interface and 8-bit parallel interface
- Contains a 16-dot common driver and a 60-dot segment driver
- Contains CGROM with character fonts of (5 x 7 dots) x 256
- Built-in bias voltage generator circuit
- Built-in contrast adjusting circuit
- Built-in 32.768 kHz crystal oscillator circuit
- Provided with 120 dot arbitrators
- 1/9 duty mode (1 line : characters, 2 lines : arbitrators)
  1/16 duty mode (2 lines : characters, 2 lines : arbitrators)
- Character blink operation can be switched between all-character lighting-on mode and all-character lighting-off mode.
- Package:
  TCP mounting with 35 mm wide film ; Tin-plated (Product name : MSM9000B-xx AV-Z-xx)
  Chip (Product name : MSM9000B-xx)
  xx indicates code number.

## BLOCK DIAGRAM



## PIN CONFIGURATION




**Pin Configuration Viewed From Pattern**

## PIN DESCRIPTIONS

| Function | Symbol | Number of Pins | Type | Description |
|---|---|---|---|---|
| CPU Interface | $\overline{CS}$ | 1 | I | Chip select input signal |
| | $\overline{WR}$ | 1 | I | Write enable signal, latch for serial interface |
| | $\overline{RD}$ | 1 | I | Read enable signal |
| | C/$\overline{D}$ | 1 | I | Command/Data select input signal |
| | DB0-7 | 8 | I/O | 8-bit parallel data inputs/outputs |
| | SI | 1 | I | Serial data input |
| | SO | 1 | O | Serial data output |
| | $\overline{SHT}$ | 1 | I | Shift clock input for data input in serial interface mode |
| Oscillation | XT | 1 | I | Crystal oscillation input, clock input |
| | $\overline{XT}$ | 1 | O | Crystal oscillation output |
| Control Signal | $\overline{P}$/S | 1 | I | Parallel/Serial interface switching signal input |
| | 9D/$\overline{16D}$ | 1 | I | Duty select signal input |
| | 32K/$\overline{EXT}$ | 1 | I | Clock select signal input |
| | $\overline{RESET}$ | 1 | I | Reset is performed by setting the $\overline{RESET}$ input to "L" level |
| | N1, N2 | 2 | I | Contrast control signal input |
| | TEST | 1 | I | Test signal input. Fix to "L" Level or leave open |
| LCD Driving Output | SEG1-SEG60 | 60 | O | Segment outputs for LCD driving |
| | COM1-COM16 | 16 | O | Common outputs for LCD driving |
| Power Supply | $V_{DD}$ | 1 | — | Positive + power supply pin for LOGIC |
| | $V_{SS}$ | 1 | — | GND pin |
| | $V_{SS1}$, $V_{SS2, 3}$ $V_{SS4}$, $V_{SS5}$ | 4 | — | Boosted voltage output pins & bias power supply pins |
| | $V_{SS6}$ | 1 | — | Voltage multiplier output pin (3-/2-fold) |
| | $V_{SH}$ | 1 | — | Haver output pin |
| | $V_{C1}$, $V_{CC1}$ | 2 | — | Voltage multiplier (3-/2-fold) |
| | $V_{C2}$, $V_{CC2}$ | 2 | — | Voltage multiplier (4-fold) |
| | Total | 112 | | |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit | Applicable pin |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | Ta=25°C, $V_{DD}$–$V_{SS}$ | –0.3 to +4.6 | V | $V_{DD}$, $V_{SS}$ |
| Bias voltage | $V_{BI}$ | Ta=25°C, $V_{DD}$–$V_{SS5}$ | –0.3 to +7 | V | $V_{DD}$, $V_{SS5}$ |
| Input voltage | $V_I$ | Ta=25°C | –0.3 to $V_{DD}$ + 0.3 | V | All input pins |
| Storage temperature | $T_{STG}$ | Chip | –55 to +150 | °C | — |
| | | TCP | –30 to +85 | | |

Ta: Ambient temperature

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit | Applicable pin |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | $V_{DD}$–$V_{SS}$ | 2.5 to 3.3 | V | $V_{DD}$, $V_{SS}$ |
| Bias voltage | $V_{BI}$ | *1, $V_{DD}$–$V_{SS5}$ | 3 to 5.5 | V | $V_{DD}$, $V_{SS5}$ |
| IC source oscillation | $f_{int}$ | *2 | 26 to 47 | kHz | *3 |
| Operating temperature | $T_{op}$ | — | –30 to +85 | °C | — |

*1 $V_{DD}$ is the highest pin and $V_{SS5}$ the lowest for the bias voltage.
*2 Connect the specified capacitors to the voltage doubler and LCD bias generator.
*3 Make sure that the crystal oscillation frequency or the divided clock frequency falls within this range.

Note 1: Ensure the chip is not exposed to any light.
Note 2: The bias voltage may exceed 5.5 V at some contrast stages. Adjust the stage with software so that the bias voltage does not exceed 5.5 V.

## ELECTRICAL CHARACTERISTICS

### DC Characteristics (1)

($V_{DD}$ = 2.5 to 3.3 V, $V_{BI}$ = 3 to 5.5 V, Ta = –30 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Applicable pin |
|---|---|---|---|---|---|---|---|
| Input high voltage 1 | $V_{IH1}$ | — | $V_{DD}$–0.25 | — | $V_{DD}$ | V | XT |
| Input high voltage 2 | $V_{IH2}$ | — | 0.8$V_{DD}$ | — | $V_{DD}$ | V | Other inputs |
| Input low voltage 1 | $V_{IL1}$ | — | 0 | — | 0.55 | V | XT |
| Input low voltage 2 | $V_{IL2}$ | — | 0 | — | 0.2$V_{DD}$ | V | Other input pins |
| Input high current 1 | $I_{IH1}$ | $V_I$=$V_{DD}$ | — | — | 1 | µA | Input pins other than XT and TEST |
| Input high current 2 | $I_{IH2}$ | $V_I$=$V_{DD}$ | 10 | — | 60 | µA | TEST (pull-down resistor) |
| Input low current 1 | $I_{IL1}$ | $V_I$=0 V | –1 | — | — | µA | Input pins other than XT and TEST |
| Off leakage current | $I_{off}$ | $V_I$=$V_{DD}$/0 V | –1 | — | 1 | µA | SO and DB0 to DB7 |
| Output high voltage 1 | $V_{OH}$ | $I_O$=–500 µA | 0.9$V_{DD}$ | — | — | V | SO and DB0 to DB7 |
| Output low voltage 1 | $V_{OL1}$ | $I_O$=500 µA | — | — | 0.1$V_{DD}$ | V | SO and DB0 to DB7 |
| COM output resistance | $R_C$ | $I_O$=±50 µA | — | — | 10 | kΩ | COM1 to COM16 |
| SEG output resistance | $R_S$ | $I_O$=±20 µA | — | — | 30 | kΩ | SEG1 to SEG60 |
| Drain current 1 | $I_{DD1}$ | During operation *1 Crystal oscillation f = 32.768 kHz | — | 15 | 35 | µA | $V_{DD}$ |
| Drain current 2 | $I_{DD2}$ | During operation *1 External clock f = 32 kHz | — | 15 | 35 | µA | $V_{DD}$ |
| Drain current 3 | $I_{DD3}$ | During standby | — | — | 7 | µA | $V_{DD}$ |

*1 No output load

Note : The values in this table are assured when the chip is not exposed to light.

### DC Characteristics (2)

($V_{DD}$=0 V, $V_{SS}$=–3 V, Ta=–30 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Applicable pin |
|---|---|---|---|---|---|---|---|
| Bias voltage 1 | $-V_{SS1}$ | $-V_{SS2,3}$ = "A"V | 1/2A–0.1 | 1/2A | 1/2A+0.1 | V | $V_{SS1}$ |
| Bias voltages 2 and 3 | $-V_{SS2,3}$ | N1 = "L", N2 = "L"<br>Contrast = "5" | 1.9 | 2.2 | 2.5 | V | $V_{SS2,3}$ |
| Bias voltage 4 | $-V_{SS4}$ | $-V_{SS2,3}$ = "A"V | 3/2A–0.1 | 3/2A | 3/2A+0.1 | V | $V_{SS4}$ |
| Bias voltage 5 | $-V_{SS5}$ | $-V_{SS2,3}$ = "A"V | 2A–0.2 | 2A | 2A+0.2 | V | $V_{SS5}$ |
| Contrast pitch | $-V_{con}$ | $V_{BI}$ for each stage | 0.18 | 0.21 | 0.26 | V | — |

Note 1: Connect a 0.1 μF capacitor to the LCD bias generator.
Note 2: The values in this table are assured when the chip is not exposed to light.

### AC Characteristics

Parallel interface

($V_{DD}$=2.5 to 3.3 V, $V_{BI}$=3 to 5.5 V, Ta=–30 to +85°C)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\overline{RD}$ high-level width | $t_{WRH}$ | — | 200 | — | ns |
| $\overline{RD}$ low-level width | $t_{WRL}$ | — | 200 | — | ns |
| $\overline{WR}$ high-level width | $t_{WWH}$ | — | 200 | — | ns |
| $\overline{WR}$ low-level width | $t_{WWL}$ | — | 200 | — | ns |
| $\overline{WR}$-$\overline{RD}$ high-level width | $t_{WWRH}$ | — | 200 | — | ns |
| $\overline{CS}$ or C/$\overline{D}$ setup time | $t_{AS}$ | — | 50 | — | ns |
| $\overline{CS}$ or C/$\overline{D}$ hold time | $t_{AH}$ | — | 0 | — | ns |
| Write data setup time | $t_{DSW}$ | — | 50 | — | ns |
| Write data hold time | $t_{DHW}$ | — | 50 | — | ns |
| Read data output delay time | $t_{DDR}$ | $C_L$=50 pF | — | 200 | ns |
| Read data hold time | $t_{DHR}$ | — | 20 | — | ns |
| External clock high-level width | $t_{WCH}$ | — | 1 | — | μs |
| External clock low-level width | $t_{WCL}$ | — | 1 | — | μs |
| $\overline{RESET}$ pulse width | $t_{WRE}$ | — | 2.0 | — | μs |
| Rise and fall time of external clock | $t_r$, $t_f$ | — | — | 100 | ns |

Note: The values in this table are assured when the chip is not exposed to light.

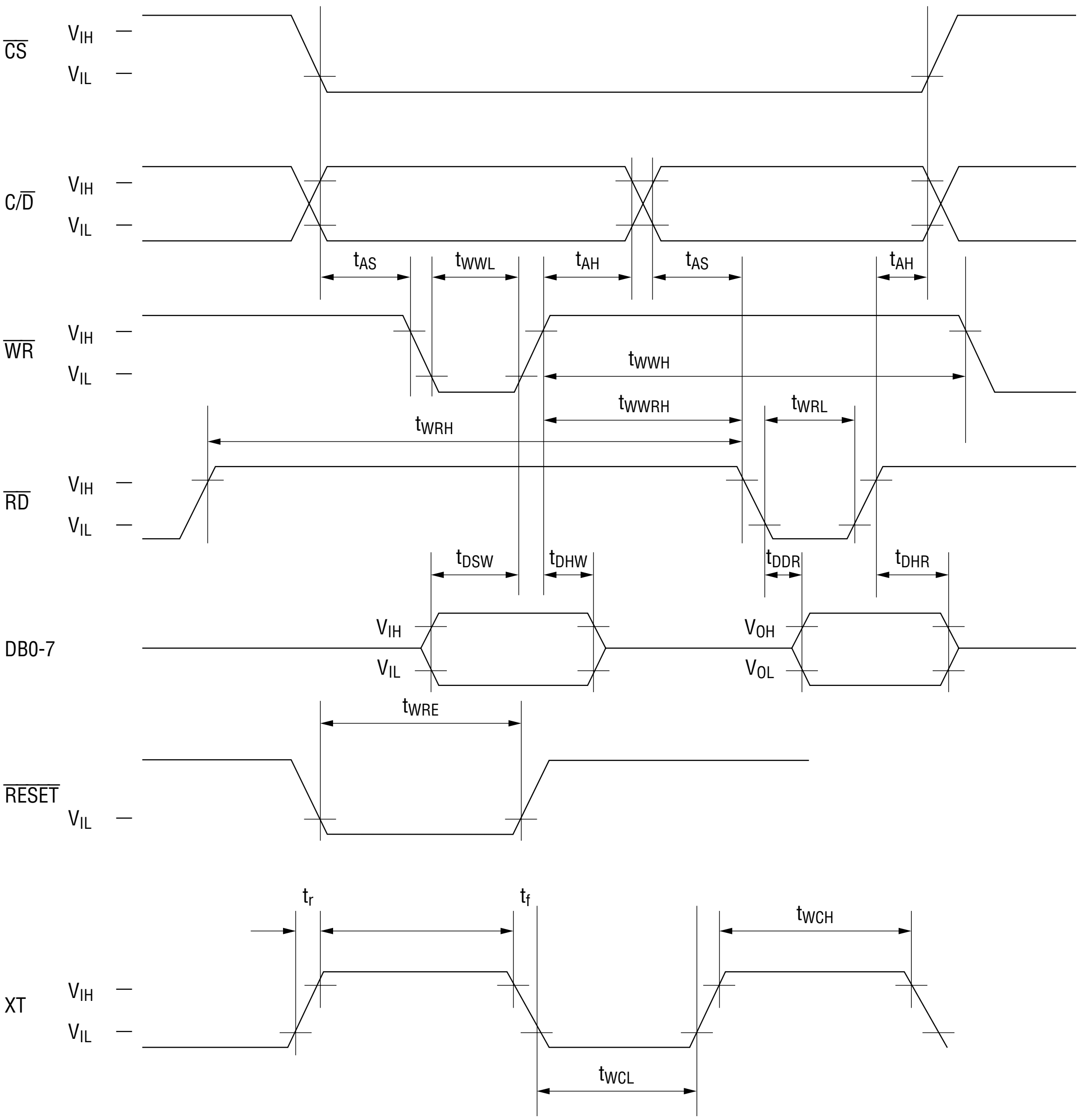
Serial interface

($V_{DD}$ = 2.5 to 3.3 V, $V_{BI}$ = 3 to 5.5 V, Ta = –30 to +85°C)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\overline{CS}$ or C/$\overline{D}$ setup time | $t_{SAS}$ | — | 100 | — | ns |
| $\overline{CS}$ or C/$\overline{D}$ hold time | $t_{SAH}$ | — | 20 | — | ns |
| SI setup time | $t_{IS}$ | — | 100 | — | ns |
| SI hold time | $t_{IH}$ | — | 20 | — | ns |
| $\overline{SHT}$ high-level pulse width | $t_{WSHH}$ | — | 100 | — | ns |
| $\overline{SHT}$ low-level pulse width | $t_{WSHL}$ | — | 100 | — | ns |
| $\overline{SHT}$ clock cycle time | $t_{SYS}$ | — | 400 | — | ns |
| SO ON delay time | $t_{ON}$ | $C_L$= 50 pF | — | 200 | ns |
| SO output delay time | $t_{DS}$ | $C_L$= 50 pF | 0 | 200 | ns |
| SO OFF delay time | $t_{OFF}$ | — | — | 100 | ns |
| BUSY delay time | $t_{BUSY}$ | $C_L$= 50 pF | — | 200 | ns |
| $\overline{WR}$ setup time | $t_{SHS}$ | — | 200 | — | ns |
| $\overline{WR}$ low-level pulse width | $t_{WWL}$ | — | 120 | — | ns |
| $\overline{RESET}$ pulse width | $t_{WRE}$ | — | 2.0 | — | µs |
| Rise and fall time of external clock | $t_r$, $t_f$ | — | — | 100 | ns |

Note: The values in this table are assured when the chip is not exposed to light.

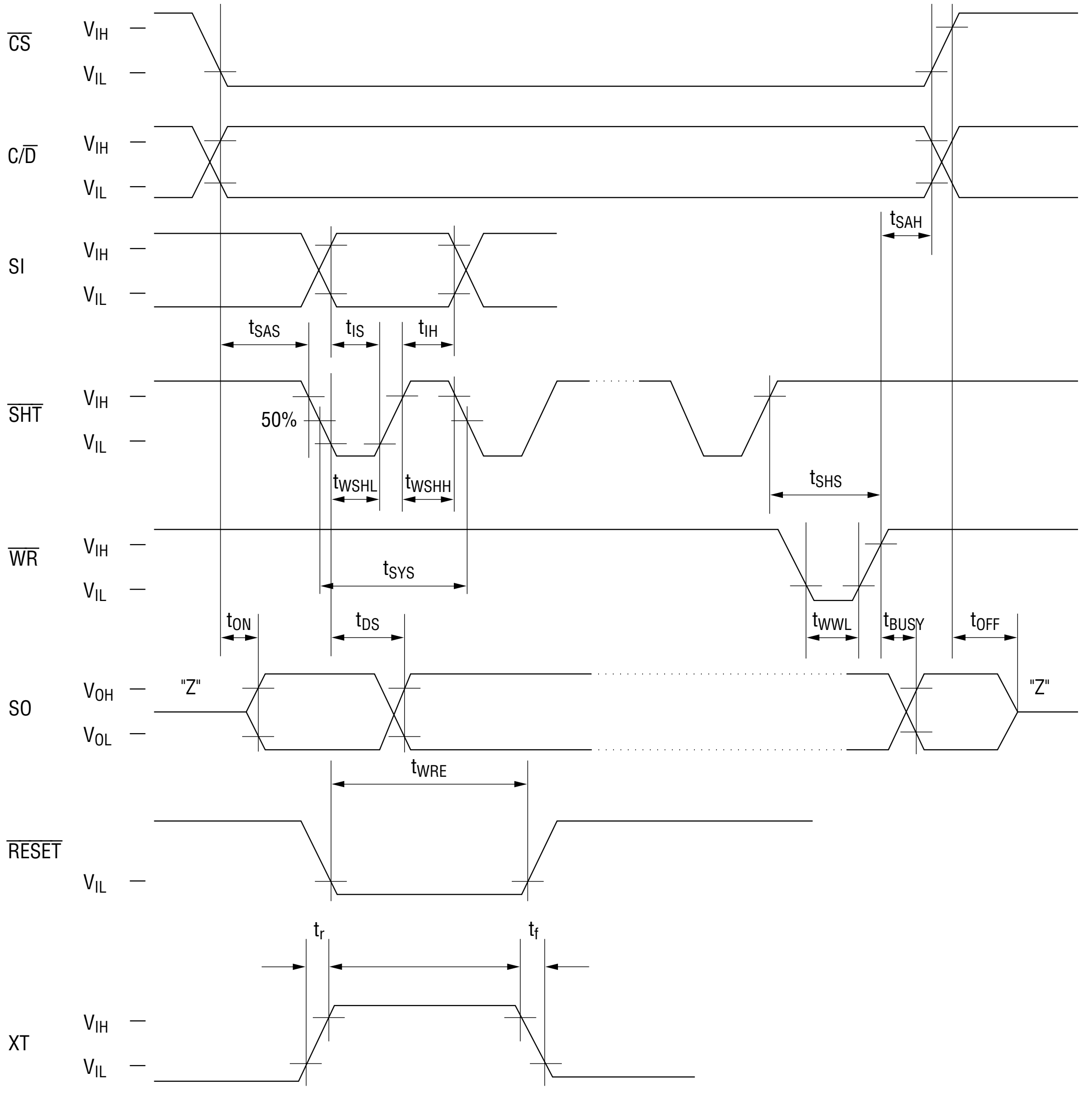
## Timing Diagram for the Parallel Interface




$V_{IH} = 0.8V_{DD}$, $V_{IL} = 0.2V_{DD}$

$V_{OH} = 0.9V_{DD}$, $V_{OL} = 0.1V_{DD}$

## Timing Diagram for the Serial Interface




$V_{IH} = 0.8\ V_{DD}$, $V_{IL} = 0.2\ V_{DD}$

$V_{OH} = 0.9\ V_{DD}$, $V_{OL} = 0.1\ V_{DD}$

# FUNCTIONAL DESCRIPTION

## Pin Functional Description

- $\overline{CS}$ (Chip Select)
  Chip select input pin. A logic low on the $\overline{CS}$ input selects the chip and a logic high on the CS input does not select the chip. Command and display data inputs can be enabled only when the chip is selected.
  When the input is high, the SO pin and DB0 to DB7 pins are in the high impedance state, causing $\overline{SHT}$, $\overline{WR}$ and $\overline{RD}$ pins high level internally.

- $\overline{WR}$ (Write Enable)
  When the parallel interface is used, this pin is the write signal input. Data is written into the register at the rising edge of $\overline{WR}$ pulse. When the serial interface is used, this pin is the latch signal input. This pin is normally high.

- $\overline{RD}$ (Read Enable)
  When the parallel interface is used, this pin is the read signal input. While the pulse is low, data can be read. The pin is normally high. When this pin is made low with C/$\overline{D}$ set low, the display data pointed to by the address pointer is output from DB0 to DB7. When the pin is made low with C/$\overline{D}$ set high, busy data is output from DB0 and low signals are output from DB1 to DB7. After the rising edge of $\overline{WR}$, busy data (H) is output. The data automatically changes to non-busy (L) after the specified time elapses.
  When the serial interface is used, fix this pin to "H" or "L".

- C/$\overline{D}$ (Command/Data Select)
  This input pin selects whether the data to be input to the SI pin and the DB7 to DB0 pins is handled as a command or display data, depending on the state of the pin at the rising edge of $\overline{WR}$. When the pin is H, the input data is handled as a command. When the pin is L, display data is input.

- DB0 to DB7 (Data Buses 0 to 7)
  Data input and output pins for the parallel interface. Normally data buses 0 to 7 are in high impedance, when $\overline{RD}$ is driven low, display data and the busy signal are output.
  When the serial interface is used, leave this pin open.

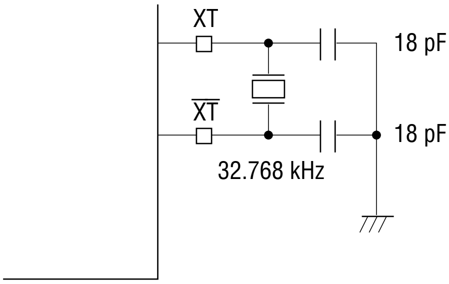
- SI (Serial Data Input)
  Data input pin for the serial interface. Commands and display data are read at the rising edge of $\overline{SHT}$ and written to registers at the rising edge of $\overline{WR}$. The eight-bit data immediately before the rising edge of $\overline{WR}$ is valid.
  When the parallel interface is used, fix this pin to "H" or "L".

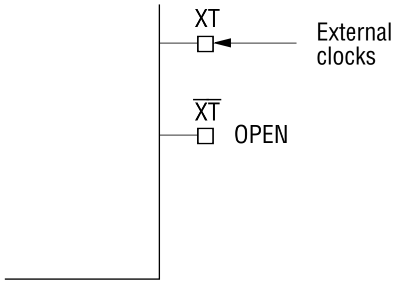
- SO (Serial Data Output)
  Data output pin for the serial interface. The display data pointed to by the address pointer is output at the rising edge of $\overline{SHT}$. After the rising edge of $\overline{WR}$, busy data (H) is output.
  The data automatically changes to non-busy (L) after the specified time elapses.
  When the parallel interface is used, this pin remains in the high impedance state.

- $\overline{SHT}$ (Shift Clock)
  Clock input pin to input and output serial interface data. Data input is synchronous with the rising edge of the clock, and the data output is synchronous with the falling edge of the clock.
  This pin is normally high.
  When the parallel interface is used, fix this pin to "H" or "L".

• XT (Crystal)
Input pin for crystal oscillation. By connecting a 32.768-kHz crystal and capacitors to this pin and the XT pin, a crystal oscillation circuit is formed. When an external clock is used, input the clock to the XT pin.

• $\overline{\text{XT}}$ (Crystal)
Output pin for crystal oscillation. By connecting a 32.768-kHz crystal and capacitors to this pin and the XT pin, a crystal oscillation circuit is formed. When the external clock is used, leave this pin open.




**Oscillation circuit diagram**

• $\overline{\text{P}}$/S (Parallel/Serial Select)
Input pin to choose between the parallel interface and serial interface. To select the parallel interface, make this pin low. To select the serial interface, make this pin high. After power is turned on, do not change the setting of this pin.

• 9D/$\overline{\text{16D}}$ (Duty Select)
Input pin to set a duty cycle. When this pin is set to "H", a duty cycle of 1/9 is selected. When the pin is set to "L", a duty cycle of 1/16 is selected. Choose either according to the panel to be used. When a duty cycle of 1/9 is chosen, leave common output pins COM10 to COM16 open.

• 32K/$\overline{\text{EXT}}$ (Clock Select)
Input pin to choose crystal oscillation mode or external clock input mode. Leave this pin at a "L" level.

• $\overline{\text{RESET}}$ (Reset)
Reset signal input pin. Setting this pin to L results in the initial state. For modes and the display after a reset input, see "Mode Settings after a Reset Input".

• N1, N2 (Contrast Change)
Input pins that determine the voltages of $V_{SS2}$ and $V_{SS3}$ together with contrast adjustment by a command. The table below shows the relationships between pin states and contrast adjustment ranges.

| N1 | N2 | Contrast adjustment range by command |
|---|---|---|
| L | L | 0 to 7 |
| L | H | 1 to 8 |
| H | L | 2 to 9 |
| H | H | 3 to A |

- TEST (Test Signal)
  Test signal input pin provided for test by the manufacturer. Fix this pin to L or leave it open.

- SEG1 to SEG60 (Segment 1 to Segment 60)
  Segment signal output pins to drive the LCD. Leave the unused pins open.

- COM1 to COM16 (Common 1 to Common 16)
  Common signal output pins to drive the LCD. When the duty cycle is 1/9, use COM1 to COM9 and leave COM10 to COM16 open.

- $V_{DD}$
  Power supply pin to the logic section. Connect this pin to the positive terminal on the power supply.

- $V_{SS}$
  Pin to be connected to the GND power supply.

- $V_{SS1}$, $V_{SS4}$, $V_{SS5}$
  Pins for voltage multiplier outputs and LCD power supply. Connect capacitors of 0.1 μF between these pins and $V_{DD}$ for the charge distribution with $V_{SS2,\,3}$ capacitor and for voltage stabilization during generation of LCD bias voltages. The logical values of the LCD bias voltage are as follows:

  Highest voltage: $V_{DD}$
  $V_{SS1}=V_{SS2,\,3}/2$
  $V_{SS2,\,3}$
  $V_{SS4}=V_{SS2,\,3}+V_{SS2,\,3}/2$
  Lowest voltage: $V_{SS5}=V_{SS2,\,3}+V_{SS2,\,3}/2+V_{SS2,\,3}/2$

  For both the 1/9 and 1/16 duty, 1/4 bias is used.

- $V_{SS2,\,3}$
  Voltage regulator output pin & LCD bias generator input used as a reference voltage for the LCD bias generator.
  Connect a capacitor of 0.1 μF between this pin and $V_{DD}$ for charge distribution among capacitors and voltage stabilization during generation of various LCD bias voltages.

- $V_{SS6}$
  Pin to connect the capacitor to store the 3-/2-fold voltage. Connect a capacitor of 0.1μF or more between this pin and $V_{DD}$.

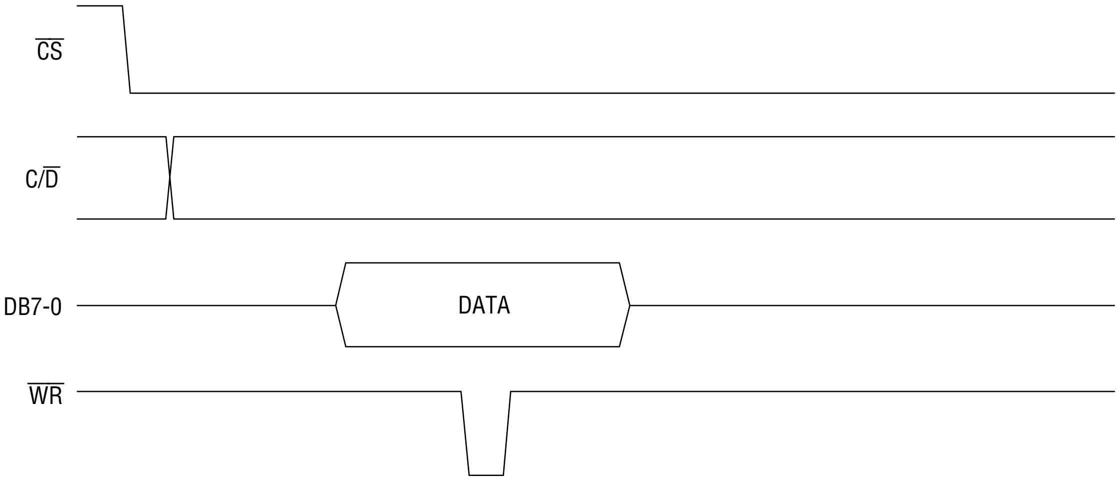
- $V_{SH}$
  Halves output pin for the voltage multiplier(3-/2-fold). Connect a 0.1 μF capacitor between this pin and $V_{DD}$.

- $V_{C1}$, $V_{CC1}$
  Pins to connect the charge distribution capacitor used for the voltage malitiplier (3-/2-fold). Connect a 0.1 µF capacitor between $V_{C1}$ and $V_{CC1}$.

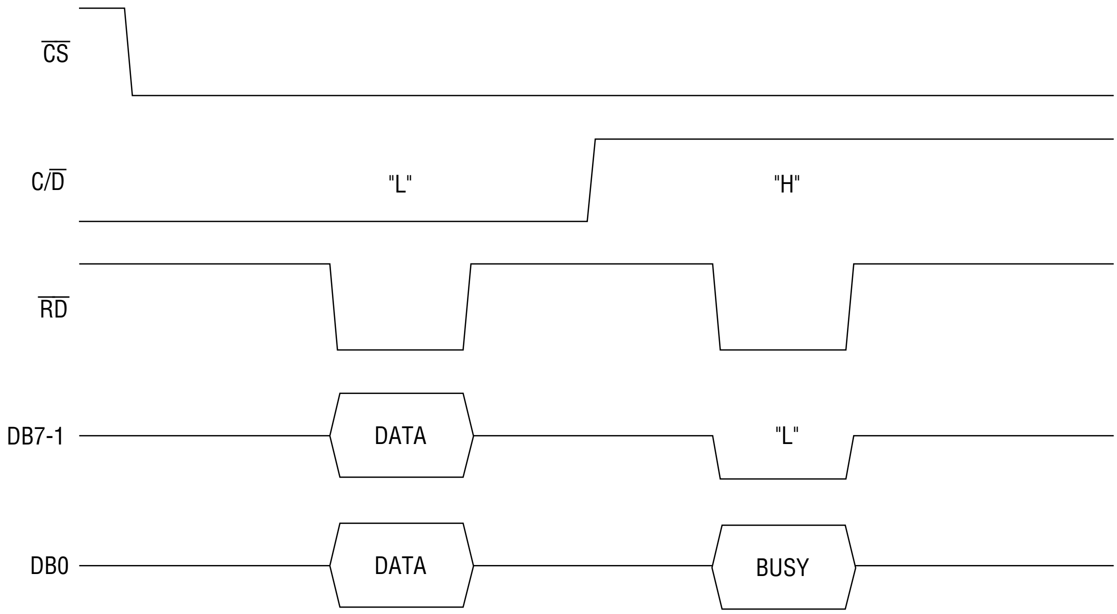
- $V_{C2}$, $V_{CC2}$
  Pins to connect the capacitor for charge distribution to generate LCD bias voltages on the basis of $V_{SS2, 3}$. Connect a 0.1 µF capacitor between $V_{C2}$ and $V_{CC2}$.

## Parallel Interface Input-Output Timing

Input timing diagram



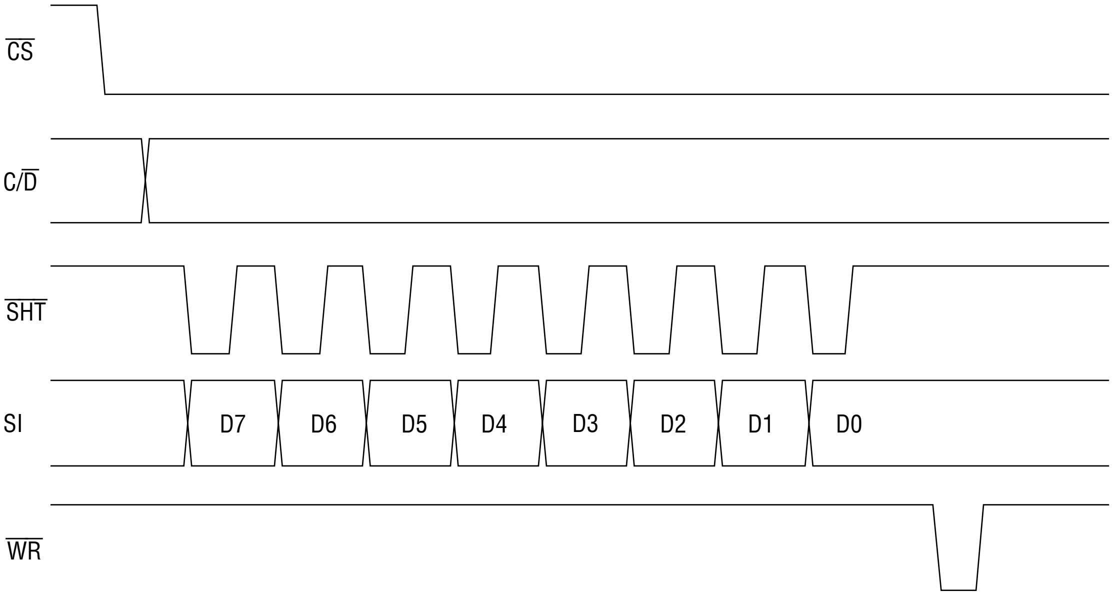

Output timing diagram



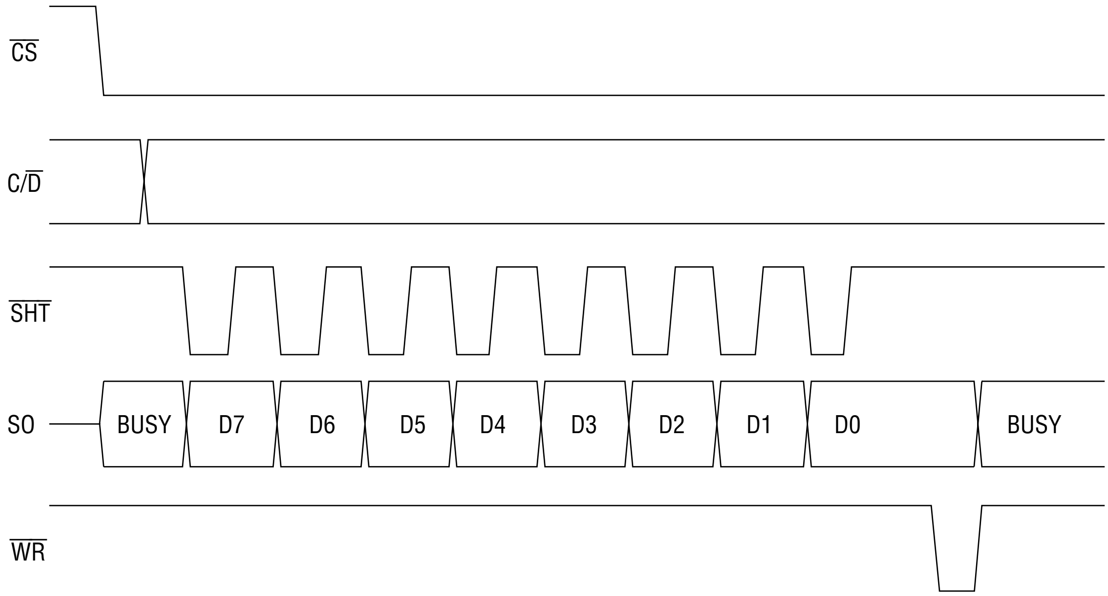

When C/$\overline{D}$="L", RAM display data is output on DB7-0 pins.
When C/$\overline{D}$="H" and DB7-1="L", busy data is output on DB0 pin.

## I/O Timings on the Serial Interface

Input timing diagram




Output timing diagram




In SO output, the eight bits after the WR pulse is input are valid.

## LIST OF COMMANDS

*: Don't Care

| No | Mnemonics | Operation | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | LPA | Load Pointer Address | 1 | 1 | A5 | A4 | A3 | A2 | A1 | A0 | Addresses 0-11, 16-27 for characters and addresses 32-43, 48-59 for arbitrators |
| 2 | LOT | Load Option | 1 | 0 | 1 | 1 | * | * | I1 | I0 | Sets additional functions during execution of AINC. |
| 3 | SF | Set Frequency | 1 | 0 | 1 | 0 | * | * | F1 | F0 | Sets conditions on master frequency. |
| 4 | BKCG 1/0 | Bank Change 1/0 | 1 | 0 | 0 | * | 0 | 0 | 0 | 1/0 | Valid only in 1/9 duty.<br>Changes display addresses 0-11, 16-27. |
| 5 | CONT U/D | Contrast Up/Down | 1 | 0 | 0 | * | 0 | 0 | 1 | 1/0 | Adjusts VLCD to 8 stages.<br>Adjustment range is changed by setting N1 and N2 pins.<br>Contrast level is up if D0="1".<br>Contrast level is down if D0="0". |
| 6 | STOP | Set Stop Mode | 1 | 0 | 0 | * | 0 | 1 | 0 | 0 | This mode is cancelled if D0="1" irrespective of either "H" or "L" on C/$\overline{D}$.<br>Stops oscillation and performs operation equivalent to that of the DISP OFF command. |
| 7 | SOE/D | Serial Out Enable/Disable | 1 | 0 | 0 | * | 0 | 1 | 1 | 1/0 | Switches between output and high impedance of SO. |
| 8 | DISP | Display On/Off | 1 | 0 | 0 | 1/0 | 1 | 0 | 0 | 1/0 | Display is ON if D0="1". Display is OFF if D0=0.<br>All commons and segments are at $V_{DD}$ level if display is OFF.<br>Arbitrators alone are displayed if D4="1". |
| 9 | AINC | Address Increment | 1 | 0 | 0 | * | 1 | 0 | 1 | * | Pointer address is incremented by 1.<br>But, this command is invalid to operations that are added by setting (I1, I0). |
| 10 | ABB | Arbitrator Blink | 1 | 0 | 0 | * | 1 | 1 | 0 | 1/0 | Data that is input after setting D0="1", is set as data for arbitrator blink (1-dot unit).<br>This is cancelled by D0="0". |
| 11 | CHB | Character Blink | 0 | 0 | 0 | * | 0 | 0 | 1/0 | * | Controls blinking of character. |
| 12 | BPC | Blink Pattern Control | 1 | 0 | 0 | * | 1 | 1 | 1 | 1/0 | Sets blink patterns of characters.<br>(□: chara) if D0="1", (■: chara) if D0="0". |
| 13 | ABLC | Arbitrator Line Change | 0 | 1 | 1 | * | * | * | L1 | L0 | Sets arbitrator display lines. |

Notes :1 Pointer address is not changed even if commands numbers 1 to 8, 10, 12, 13 are enterd.
:2 Pointer address is automatically incremented by 1 when commands numbers 9, 11, display code data, and arbitrator data are enterd.

- **LOT**

| I1 | I0 | Additional function | Remarks |
|---|---|---|---|
| 0 | 0 | No additional function | |
| 0 | 1 | A blank code is written for each subsequent AINC. | Used to automatically clear RAM at power-on. |
| 1 | 0 | Blinking is canceled for each subsequent AINC. | |
| 1 | 1 | The above two functions are ORed. | |

- **SF**

| F1 | F0 | Frequency of source oscillation in the IC | Remarks |
|---|---|---|---|
| 0 | 0 | XT | Used to generate the optimum frequency when external clocks are input. |
| 0 | 1 | XT ÷ 2 | |
| 1 | 0 | XT ÷ 4 | |
| 1 | 1 | XT ÷ 8 | |

- **DISP**

| D4 | D0 | Character | Arbitrator | Remarks |
|---|---|---|---|---|
| * | 0 | OFF | OFF | Used to turn on and off the display. |
| 0 | 1 | ON | ON | |
| 1 | 1 | OFF | ON | |

* : Don't care

- **ABLC (when the duty is 1/16)**

| L1 | L0 | Arbitrator 1 | Arbitrator 2 | Remarks |
|---|---|---|---|---|
| 0 | 0 | COM1 | COM2 | Arbitrator 1 indicates display data at addresses 32 to 43, while arbitrator 2 indicates display data at addresses 48 to 59. |
| 0 | 1 | COM15 | COM16 | |
| 1 | * | COM16 | COM1 | |

* : Don't care

- **ABLC (when the duty is 1/9)**

| L1 | L0 | Arbitrator 1 | Arbitrator 2 | Remarks |
|---|---|---|---|---|
| 0 | 0 | COM1 | COM2 | Arbitrator 1 indicates display data at addresses 32 to 43, while arbitrator 2 indicates display data at addresses 48 to 59. |
| 0 | 1 | COM8 | COM9 | |
| 1 | * | COM9 | COM1 | |

* : Don't care

## Explanation of Commands

[D7, D6, D5, D4, D3, D2, D1, D0], X = Don't care

- LPA (Load Pointer Address)
  [1, 1, A5, A4, A3, A2, A1, A0]
  This command sets in the address pointer the address of the command to be executed or the address of the display data to be input. The settable addresses are inconsecutive addresses 00H to 0BH, 10H to 1BH, 20H to 2BH, 30H to 3BH represented by A5 to A0. When addresses 0CH to 0FH, 1CH to 1FH, 2CH to 2FH, or 3CH to 3FH are set, 00H is assumed.
  After $\overline{\text{RESET}}$ = "L", the address is set to 00H.

- LOT (Load Option)
  [1, 0, 1, 1, X, X, I1, I0]
  This command executes the additional function specified by I1 and I0 to the display of the current address when the AINC command is executed. Additional functions are shown below.
  After $\overline{\text{RESET}}$ = "L",, both I1 and I0 are set to "0".

| I1 | I0 | Additional function |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | After this command is executed, the blank code is writtern each time AINC is executed. |
| 1 | 0 | After this command is executed, blinking is canceled each time AINC is executed. |
| 1 | 1 | The above two additional functions are ORed. |

- SF (Set Frequency)
  [1, 0, 1, 0, X, X, F1, F0]
  This command sets the number by which the external clock input from the XT pin is divided in order to get the source frequency inside the IC. This command is valid when 32K/$\overline{\text{EXT}}$ pin is "L". The dividing ratio is specified by F1 and F0 in the command. The table below lists the source oscillation frequencies in the IC.
  After $\overline{\text{RESET}}$ = "L", both F1 and F0 are set to "0".

| F1 | F0 | Frequency of source oscillation in the IC |
|---|---|---|
| 0 | 0 | XT |
| 0 | 1 | XT ÷ 2 |
| 1 | 0 | XT ÷ 4 |
| 1 | 1 | XT ÷ 8 |

- BKCG1/0 (Bank Change 1/0)
  [1, 0, 0, X, 0, 0, 0, 1/0]
  This command changes addresses (banks) to be displayed. The command is valid only when the duty is 1/9. When D0 is 0, addresses 0 to 11 (character 1), 32 to 43, and 48 to 59 (arbitrators 1 and 2) are displayed. When D0 is "1", addresses 16 to 27 (character 2), 32 to 43, and 48 to 59 (arbitrators 1 and 2) are displayed. The command and display data can be set regardless of the bank setting.
  After $\overline{\text{RESET}}$ = "L", D1 is set to "0".

- CONT U/D (Contrast Up Down)
  [1, 0, 0, X, 0, 0, 1, 1/0]
  This command selects the voltage of $V_{SS2, 3}$ that is used as the reference voltage for the LCD bias. When the value of $V_{SS2, 3}$ is changed, the contrast is changed accordingly.
  The contrast is controlled by the value of the 3-bit up/down counter so that eight stages are supported. The value of the up/down counter is incremented when "1" is entered by this command and decremented when "0" is entered. The counter changes within the range of 0 to 7.
  When the counter reaches 7, it goes back to "0".
  According to the settings of N1 and N2, the contrast stages can be changed to 1 to 8, 2 to 9, or 3 to A.
  At stage 0, the bias voltage is minimized. The larger the contrast stage, the higher the bias voltage. At stage A, the bias voltage is maximized.
  After a low $\overline{\text{RESET}}$ is input, the counter is set to the minimum value specified by N1 and N2.

  Example: · · · 6↔7↔0↔1↔2↔3↔4↔5↔6↔7↔0 · · ·

  Note: At some contrast stages, the bias voltage may be increased to 5.5 V or higher. Adjust the stage so that the bias voltage does not exceed 5.5 V.

- STOP (Set Stop Mode)
  [1, 0, 0, X, 0, 0, 1, 0]
  This command sets standby mode. Specifically, the command stops the oscillation block to prevent current form flowing through the oscillation block and outputs the $V_{DD}$ level to all LCD output pins. Standby mode is canceled when D0 is set to "1" regardless of the setting of the C/$\overline{\text{D}}$ pin. When a command or data with D0 set to "1" is entered, the command is executed or the data is input. At the same time, standby mode is canceled.
  After $\overline{\text{RESET}}$ = "L", standby mode is disabled.

- SOE/D (Serial Out Enable/Disable)
  [1, 0, 0, X, 0, 1, 1, 1/0]
  This command controls the impedance of the SO output pin. The command is valid only when the serial interface is used. When D0 is set to "0", the SO pin is set in the high impedance state.
  After $\overline{\text{RESET}}$ = "L", D0 is set to "0".

- DISP (Display On/Off)
  [1, 0, 0, 1/0, 1, 0, 0, 1/0]
  This command sets LCD display mode. When D0 is set to "1", the LCD is turned on. When D0 is set to "0", the LCD is turned off, in which case, the $V_{DD}$ level is output to all segment and common pins. When the LCD is turned ON (D0="1"), and D4 is set to "1", only arbitrators are displayed and when D4 is set to "0", both characters and arbitrators are displayed. The table below lists display modes.
  After $\overline{\text{RESET}}$ = "L", both D4 and D0 are set to "0".

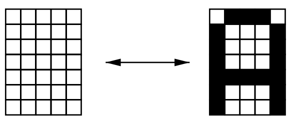
| D4 | D0 | Characters | Arbitrators |
|---|---|---|---|
| X | 0 | OFF | OFF |
| 0 | 1 | ON | ON |
| 1 | 1 | OFF | ON |

- AINC (Address Increment)
  [1, 0, 0, X, 1, 0, 1, X]
  This command increments the value of the address pointer by one. Each time this command is input, the value is incremented by one. Addresses are increased as follows: 00 to 11 → 16 to 27 → 32 to 43 → 48 to 59 → 00 ···. This cycle is repeated. The function specified by the LOT command is performed for the previous address before the address incremented by one every time this command is input.

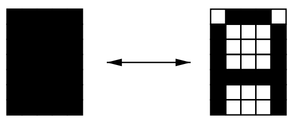
- ABB (Arbitrator Blink)
  [1, 0, 0, X, 1, 1, 0, 1/0]
  This command turns arbitrator blinking on or off. Display data input after D0 is set to "1" is handled as arbitrator blink data. Input blink data corresponds to dots of the arbitrator at the same address on a one-to-one basis. When the dot is "1", blinking is enabled. When the dot is "0", blinking is disabled. While the dot is blinking, it is turned on and off repeatedly.
  Blinking can be specified for a dot for which enabling the arbitrator is not specified, but the dot does not blink.
  Dummy data must be set for arbitrator data D5 to D7. Data cannot be written to addresses 00 to 31 and 44 to 47.
  After $\overline{RESET}$ = "L", D0 is set to "0".

- CHB (Character Blink)
  [0, 0, 0, X, 0, 1, 1/0, X]
  This command enables or disables character blinking. The command is executed for the address pointed to by the address pointer. When D1 is set to "1", blinking is enabled. When D1 is set to "0", blinking is disabled. During blinking, the turning on of all dots (5×7 dots) and character display are repeated. In another blinking pattern, the turning off of all dots and character display are repeated. Either pattern is selected by the BPC command.
  After $\overline{RESET}$ = "L", the value of the address pointer is automatically incremented by one.

- BPC (Blink Pattern Control)
  [1, 0, 0, X, 1, 1, 1, 1/0]
  This command selects a character blinking pattern. When D0 is set to "1", the turning on of all dots (5×7 dots) and character display are repeated. When D0 is set to "0", the turning off of all dots and character display are repeated.
  When D0 is "1" but the character is a blank, the character does not blink visibly. When D0 is "0", the character does not blink visibly while all its dots are turned on.
  After $\overline{RESET}$ = "L", D0 is set to "0".



[D0 = "1"]



[D0 = "0"]

• ABLC (Arbitrator Line Change)
[0, 1, 1, X, X, X, L1, L0]
This command selects a common line for arbitrator display, according to the settings of L1 and L0. The table below shows the relationships between L1 and L0 and displayed common lines, assuming that the display data at addresses 00 to 11 is character 1, the display data at addresses 16 to 27 is character 2, the display data at addresses 32 to 43 is arbitrator 1, and the display data at addresses 48 to 59 is arbitrator 2. Different common lines are displayed for 1/16 duty and 1/9 duty.
After a low $\overline{\text{RESET}}$ is input, both L1 and L0 are set to "0".
Common lines displayed by the ABLC command are as follows:

When 1/16 duty is chosen

| L1 | L0 | Character 1 | Character 2 | Arbitrator 1 | Arbitrator 2 |
|---|---|---|---|---|---|
| 0 | 0 | COM3 to 9 | COM10 to 16 | COM1 | COM2 |
| 0 | 1 | COM1 to 7 | COM8 to 14 | COM15 | COM16 |
| 1 | X | COM2 to 8 | COM9 to 15 | COM16 | COM1 |

When 1/9 duty is chosen

| L1 | L0 | Character 1 | Character 2 | Arbitrator 1 | Arbitrator 2 |
|---|---|---|---|---|---|
| 0 | 0 | COM3 to 9 | | COM1 | COM2 |
| 0 | 1 | COM1 to 7 | | COM8 | COM9 |
| 1 | X | COM2 to 8 | | COM9 | COM1 |

Note: When 1/9 duty is chosen, characters 1 and 2 can be switched by changing the bank.

• Increment of the address pointer by one
When display data or arbitrator blink data is input or the AINC or CHB command is executed, the address pointer is incremented by one.

### Mode Setting after a Reset Input

The table below lists the settings of individual modes during a $\overline{\text{RESET}}$ =L input.

| Command | Mode setting | Remarks |
|---|---|---|
| LPA | A5 to A0 = "0" | The address pointer is set to "00". |
| LOT | I1 = "0", I0 = "0" | Load Option command with no additional function. |
| SF | F1= "0", F0 = "0" | The dividing ratio is set to 1. |
| BKCG 1/0 | D0 = "0" | Display addresses 00 to 11 are set. |
| CONT U/D | — | The control counter is set to 0 (Stage 0). |
| STOP | — | Standby mode is disabled. |
| SOE/D | D0 = "0" | The SO pin is set to the high impedance state. |
| DISP | D4 = "0", D0 = "0" | Both characters and arbitrators display mode is set, but the dispaly is turned off. |
| ABB | D0 = "0" | Display data input mode is enabled. |
| BPC | D0 = "0" | Blink mode is such that the turning on of all dots and character display are repeated. |
| ABLC | L1 = "0", L0 = "0" | Arbitrator 1 corresponds to COM1, and arbitrator 2 corresponds to COM2. |

- Even when a reset is input, display RAM is not initialized. To clear the display data, a blank code must be written. (This can be done with an additional function of the AINC command.)

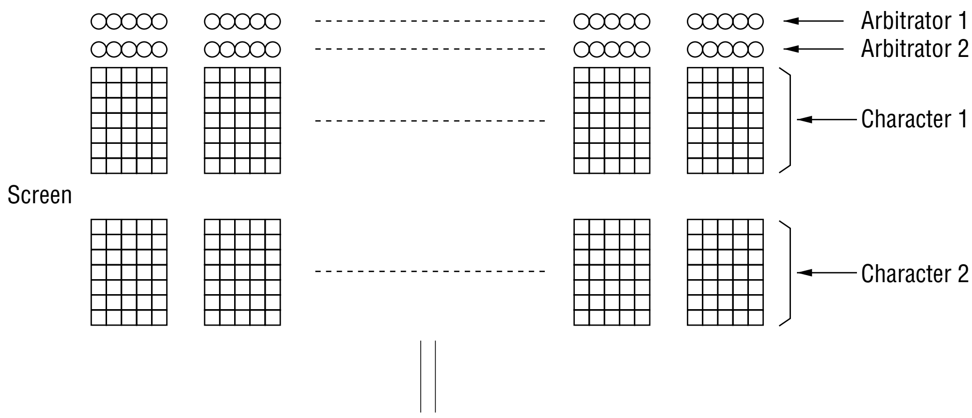
### Mode Settings during Standby

The table below lists the settings of individual modes during standby.

| Command | Mode setting | Remarks |
|---|---|---|
| LPA | A5 to A0 = "0" | The address pointer is set to "00". |
| LOT | No change | The setting before standby mode is retained. |
| SF | | |
| BKCG 1/0 | | |
| CONT U/D | — | The count before standby mode is retained. |
| STOP | — | Standby state 10. No change. |
| SOE/D | D0 = "0" | The setting before standby mode is retained. |
| DISP | D4 = "0", D0 = "0" | Both character and arbitrator display mode is set, but the display is turned off. |
| ABB | No change | The setting before standby mode is retained. |
| BPC | | |
| ABLC | | |

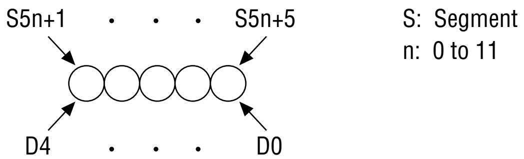
- Data before standby mode is retained in display RAM.

## Display Screen and Memory Addresses




| RAM map | | | | | | |
|---|---|---|---|---|---|---|
| | 32 | 33 | ... | 42 | 43 | ← Arbitrator 1 |
| | 48 | 49 | ... | 58 | 59 | ← Arbitrator 2 |
| | 0 | 1 | ... | 10 | 11 | ← Character 1 |
| | 16 | 17 | ... | 26 | 27 | ← Character 2 |

Note: Characters are input as codes. Arbitrators are displayed directly without intervening CG ROM. Input data is displayed as shown below.




Dummy data must be set for input data D7 to D5. Either "1" or "0" can be input as input data of D7 to D5.

## Calculation Method of Various Kinds of Frequencies

• Frame frequency

For 1/16 duty
(Source clock cycle) × (1/Dividing ratio) × 448 = Frame cycle · · · · · (1)
For 1/9 duty
(Source clock cycle) × (1/Dividing ratio) × 468 = Frame cycle · · · · · (2)

Example
Source oscillation frequency = 32.768 kHz
Dividing ratio = 1/1
Specification: 1/16 Duty
Clock cycle Ts = 30.5 µs

Under these conditions, the frame frequency can be calculated from expression (1) as follows:
Frame cycle Tf = $30.5 \times 10^{-6} \times 1 \times 448 = 13.66$ ms

Therefore
Frame frequency = 73.2 Hz

• Calculating the blinking frequency
The blinking frequency can be calculated from the following expression:

Blinking frequency = (Source clock cycle) × (1/Dividing ratio) × $2^{15}$ · · · · · (3)

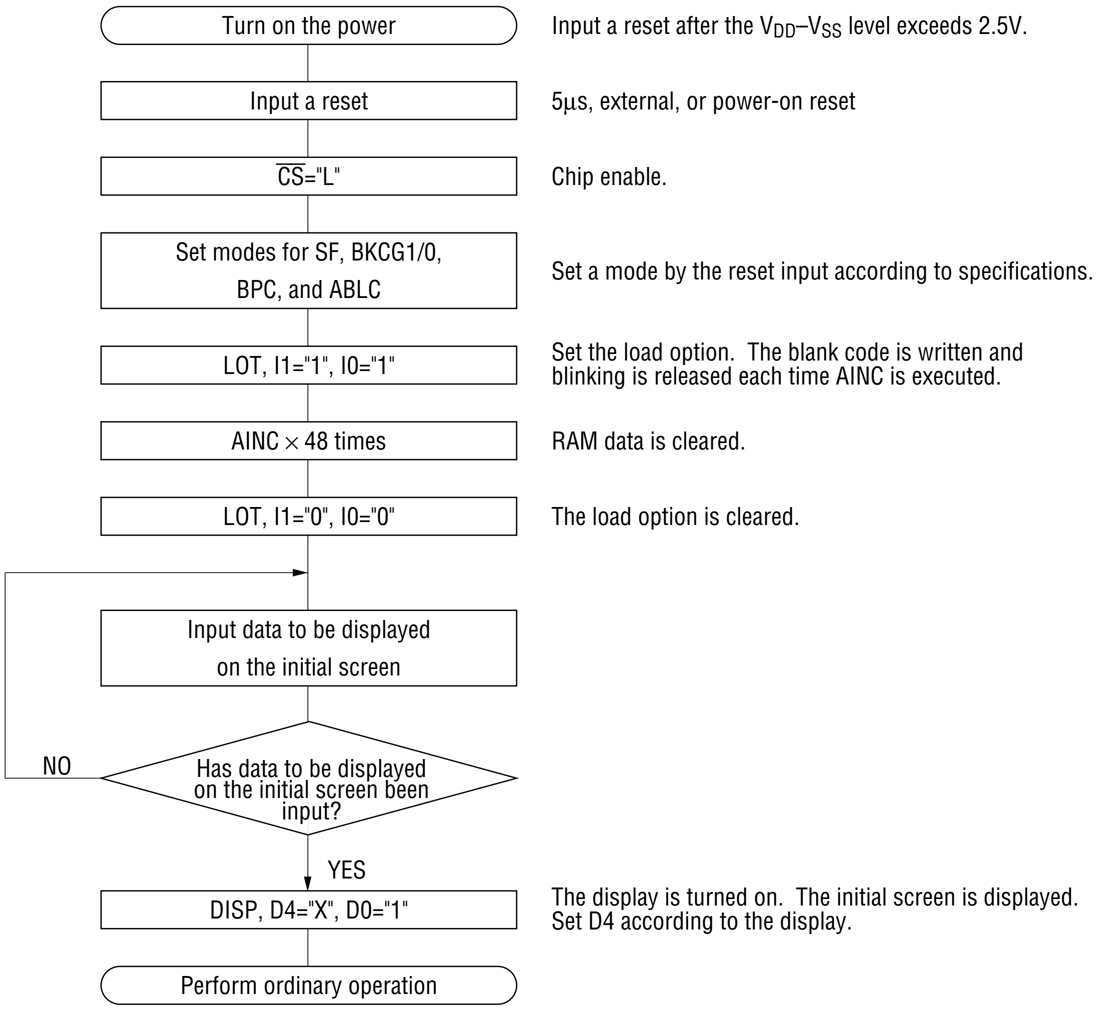
Example
Source oscillation frequency = 32.768 kHz
Dividing ratio = 1/1
Clock cycle $T_S$ = 30.5 µs

Under these conditions, the blinking frequency can be calculated from expression (3) as follows:
Blinking cycle Tf = $30.5 \times 10^{-6} \times 1 \times 2^{15} = 1$ s

Therefore
Blinking frequency = 1 Hz

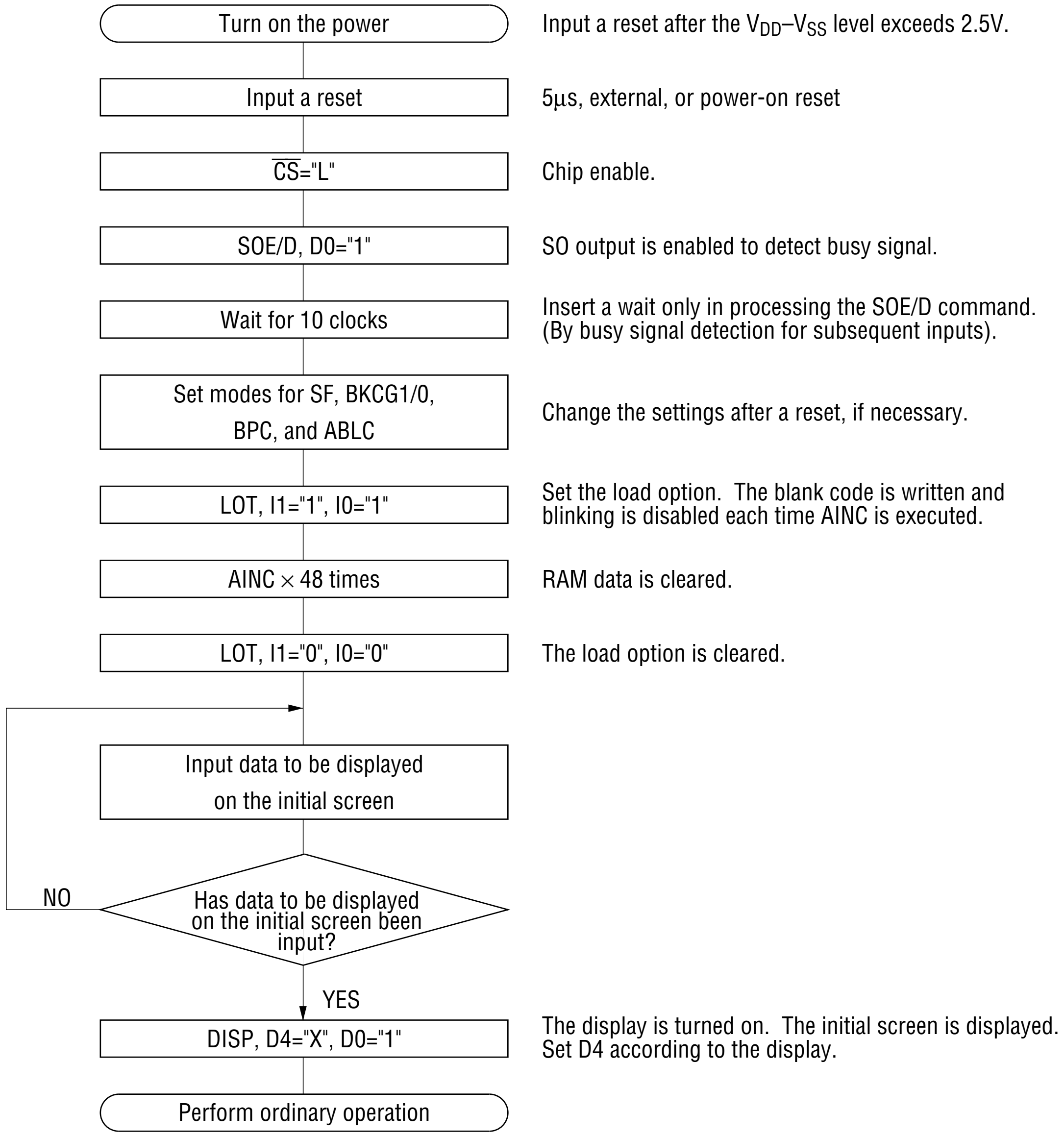
• Source oscillation frequency and busy time
When data is written to or read from RAM or a command is input, data processing time (busy time) is taken. The maximum busy time is the source clock cycle multiplied by 10. The busy signal (not-busy = "L", busy = "H" ) is detected at the SO pin when the serial interface is used or at the DB0 pin when the parallel interface is used. When display data or commands are input consecutively, a wait must be inserted for the source clock cycle multiplied by 10. Another way is to detect busy signals and input data or commands during not-busy time only.

### Flowchart at Power-on (parallel interface)



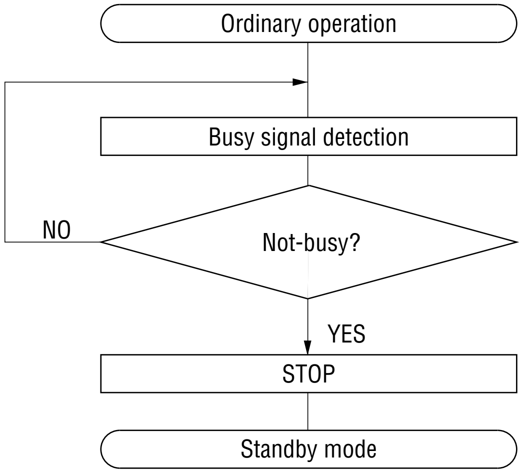

- When the stage to be selected is already determined, contrast can be adjusted before the display is turned on (for example, at the same time as when mode is set).
- After a command or display data is input, check for busy data. Make sure that the busy data ("H") has changed to not-busy data ("L") before making the next input.

## Flowchart at Power-on (serial interface)



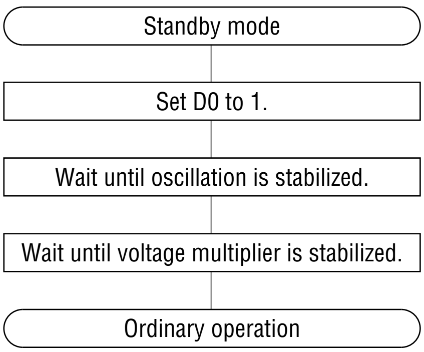

- When the stage to be selected is already determined, contrast can be adjusted before the display is turned on (for example, at the same time as when mode is set).
- After a command or display data is input, check for busy data. Make sure that the busy data ("H") has changed to not-busy data ("L") before making the next input.

## Flowcharts to Set and Cancel Standby Mode




Confirm not-busy signal.

Set standby mode.

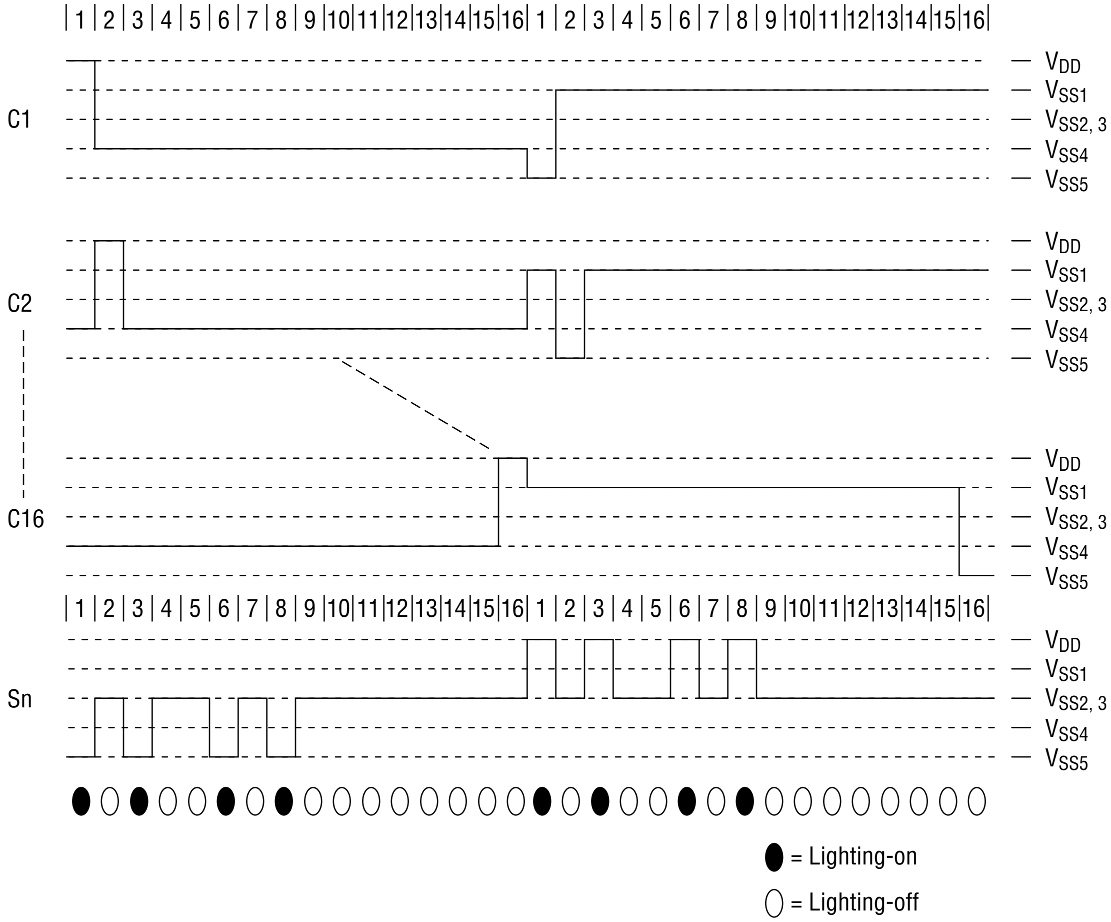



When the code in which D0 is set to 1 is input, standby mode is canceled regardless of C/D input.

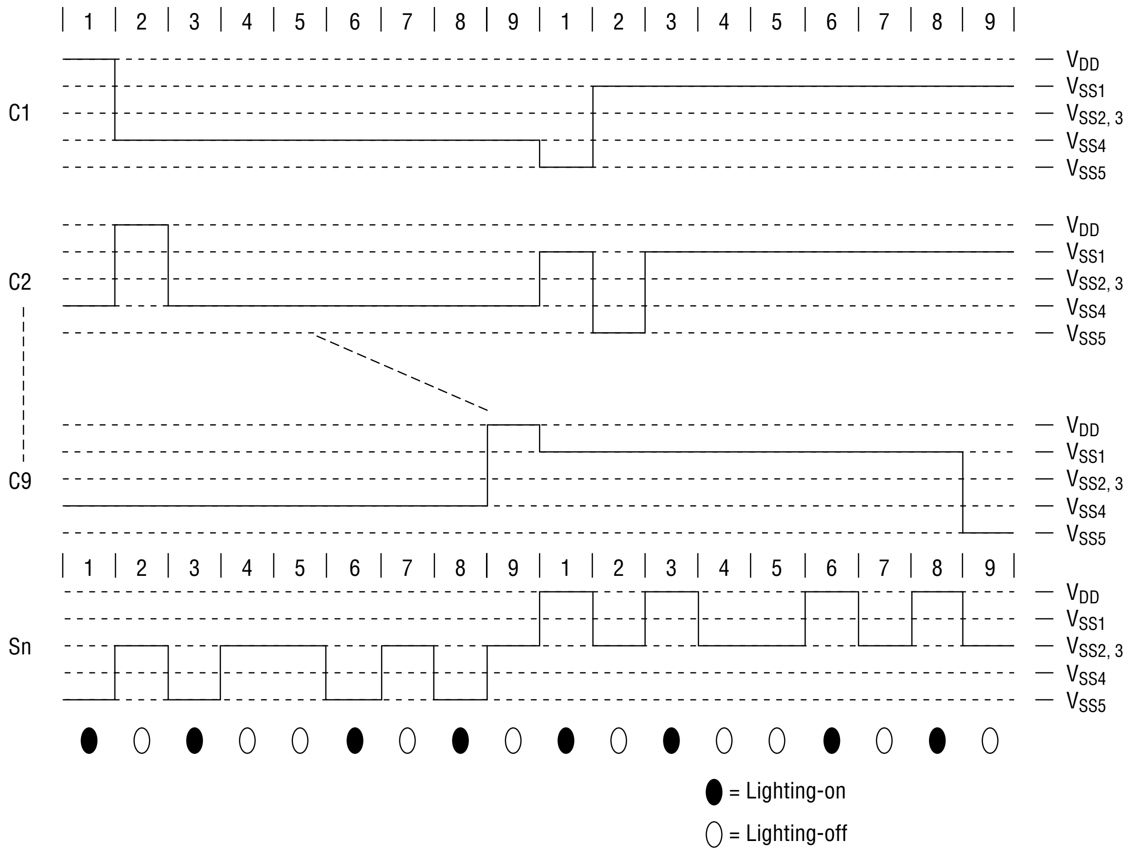
The length of the wait depends on the configuration of the oscillation circuit.

### Liquid Crystal Applied Waveform Examples

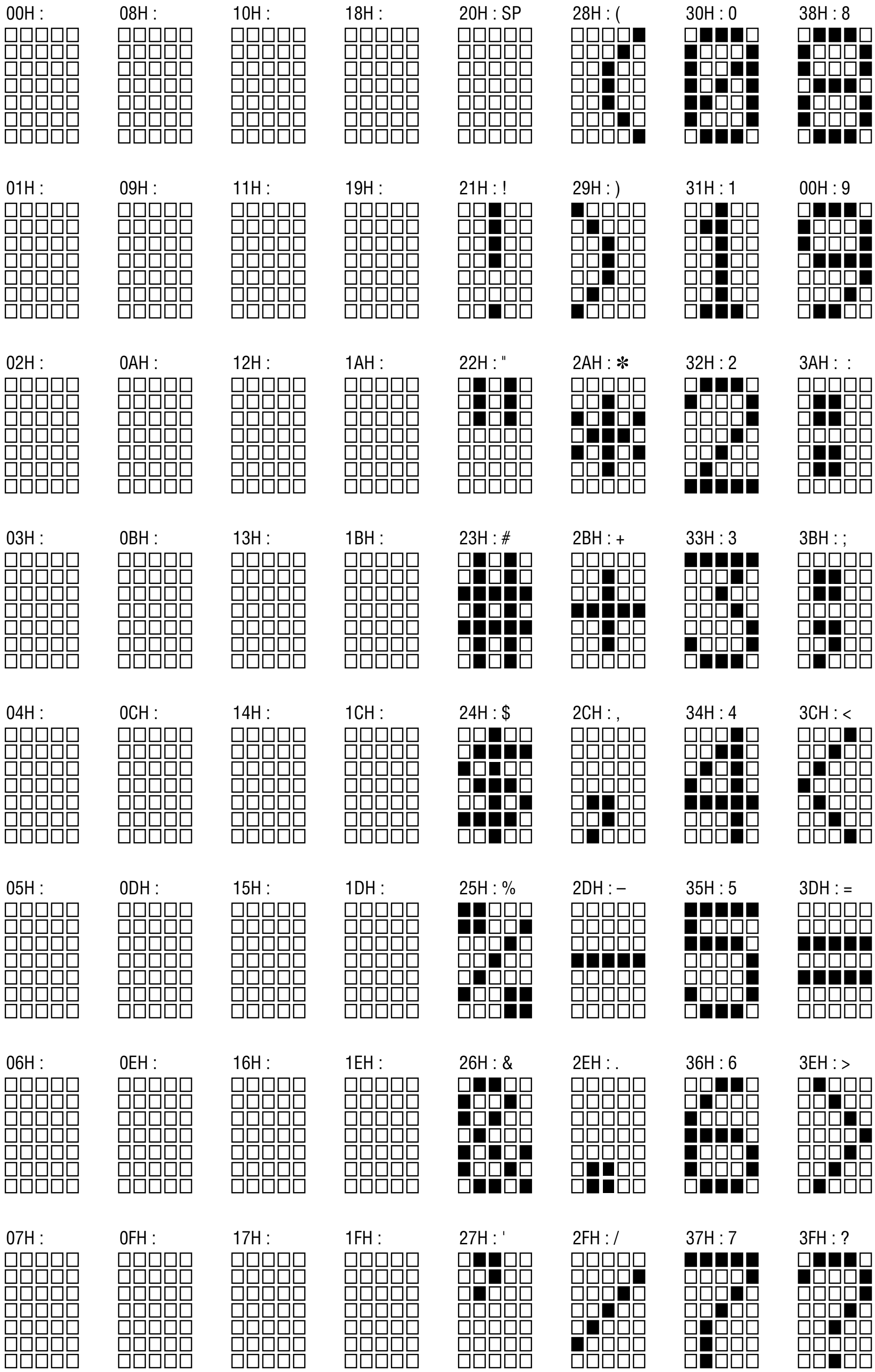
### In 1/16 duty

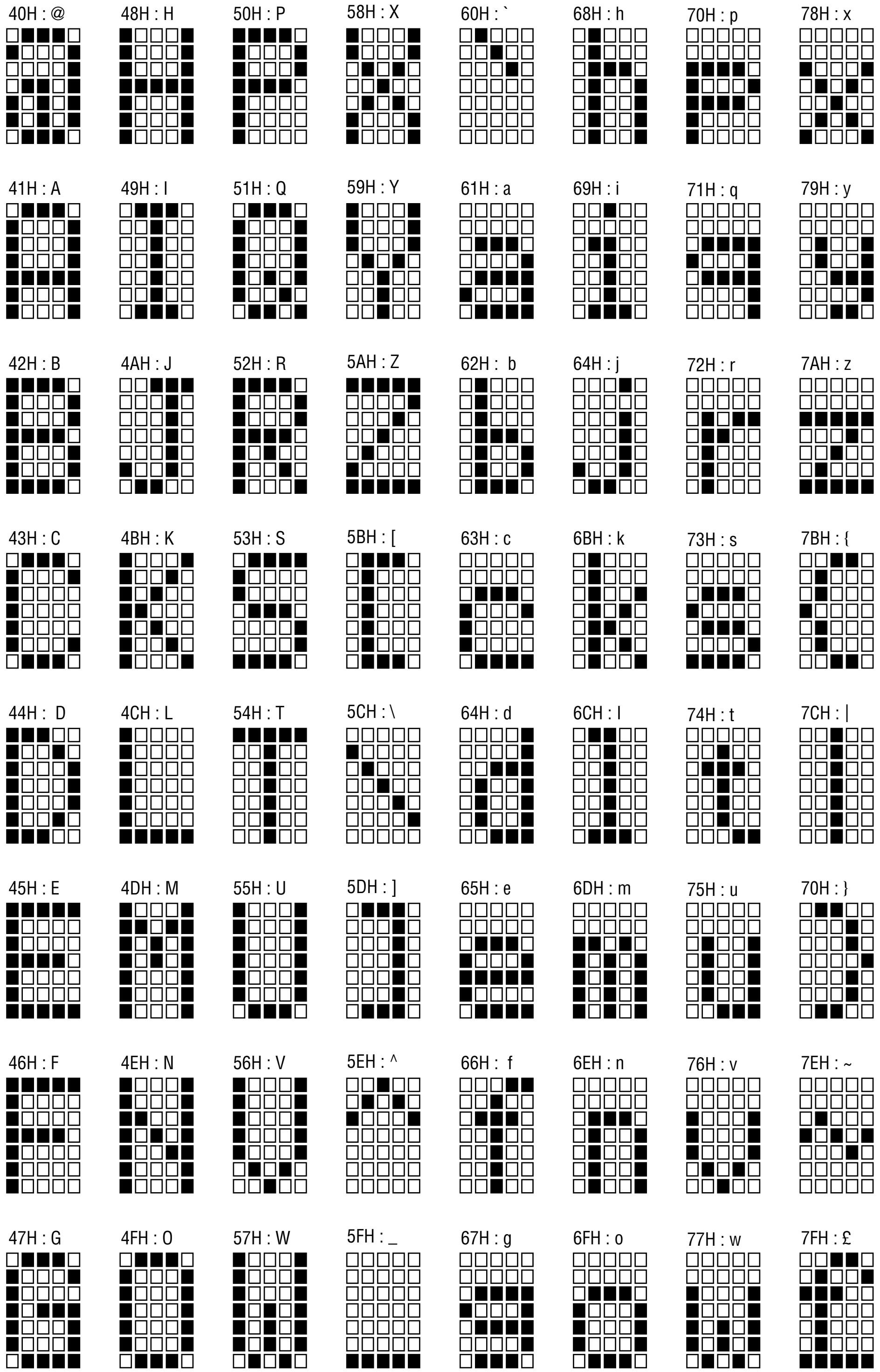


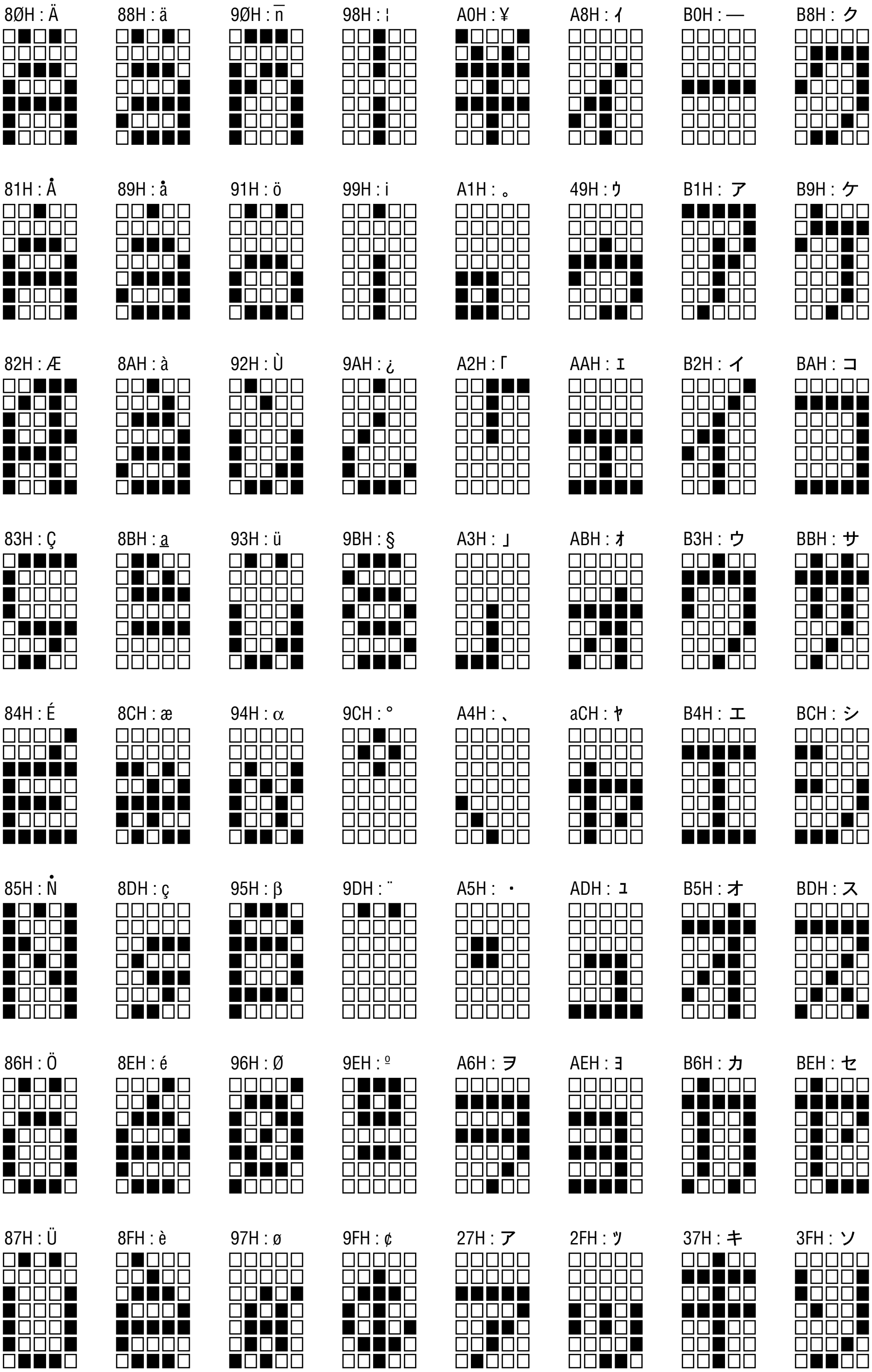
## In 1/9 duty

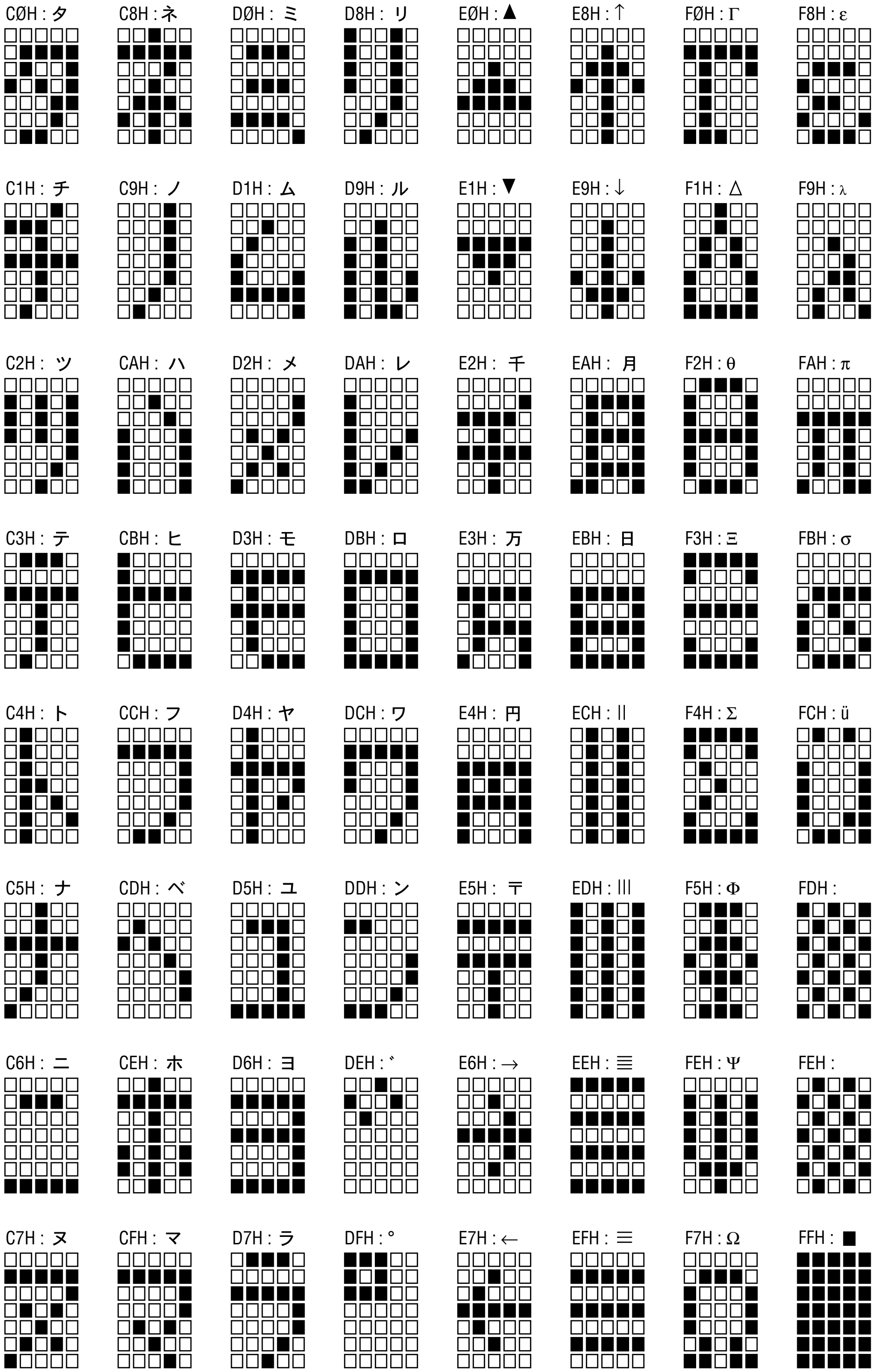

1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9
C1
C2
C9
Sn
VDD
VSS1
VSS2, 3
VSS4
VSS5
= Lighting-on
= Lighting-off

## Codes and Character Fonts of Code -01




40H : @
48H : H
50H : P
58H : X
60H : `
68H : h
70H : p
78H : x
41H : A
49H : I
51H : Q
59H : Y
61H : a
69H : i
71H : q
79H : y
42H : B
4AH : J
52H : R
5AH : Z
62H : b
64H : j
72H : r
7AH : z
43H : C
4BH : K
53H : S
5BH : [
63H : c
6BH : k
73H : s
7BH : {
44H : D
4CH : L
54H : T
5CH : \
64H : d
6CH : l
74H : t
7CH : |
45H : E
4DH : M
55H : U
5DH : ]
65H : e
6DH : m
75H : u
70H : }
46H : F
4EH : N
56H : V
5EH : ^
66H : f
6EH : n
76H : v
7EH : ~
47H : G
4FH : O
57H : W
5FH : _
67H : g
6FH : o
77H : w
7FH : £

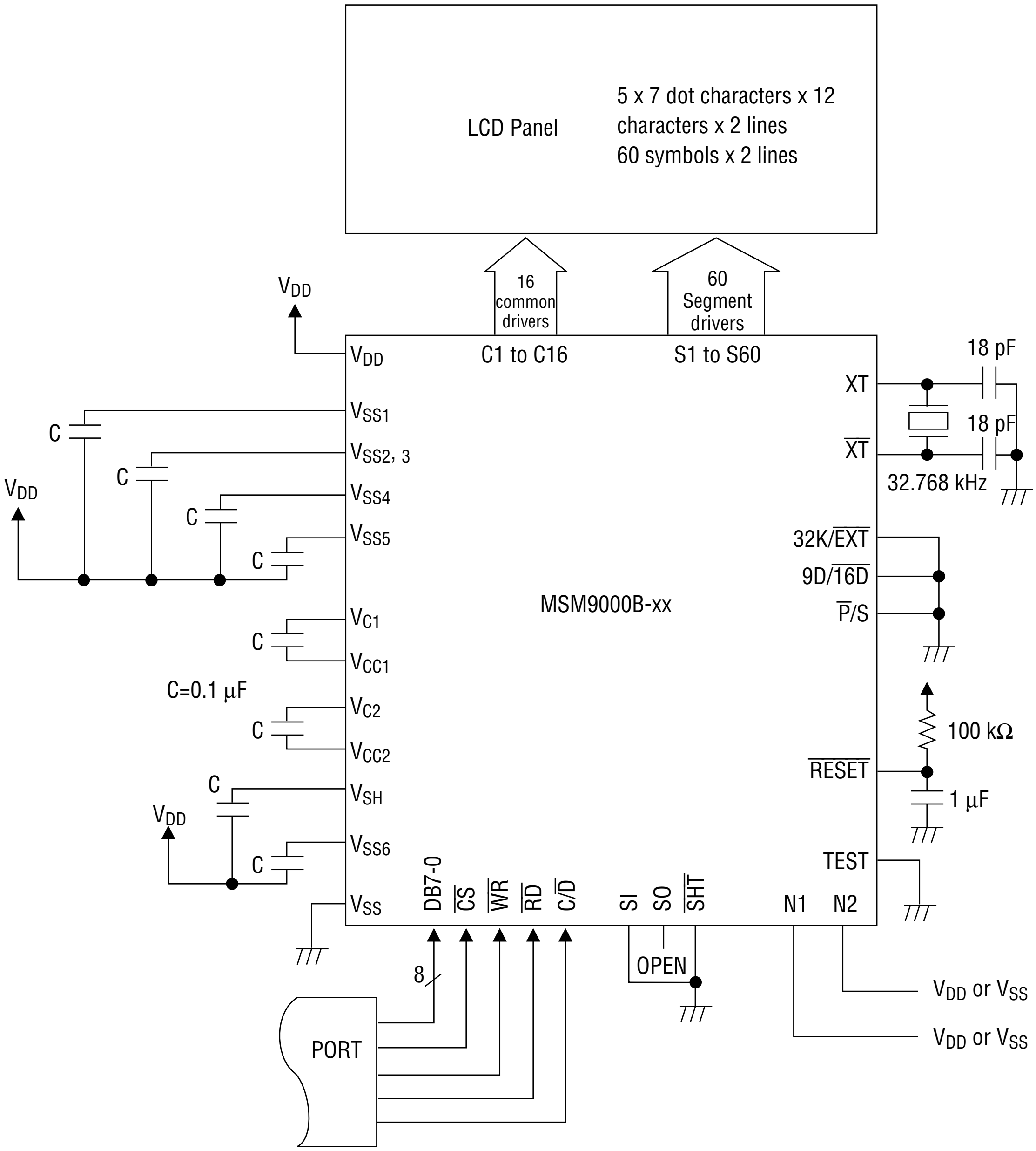

8ØH : Ä
88H : ä
9ØH : n̄
98H : ¦
A0H : ¥
A8H : ィ
B0H : —
B8H : ク
81H : Å
89H : å
91H : ö
99H : i
A1H : 。
49H : ゥ
B1H : ア
B9H : ケ
82H : Æ
8AH : à
92H : Ù
9AH : ¿
A2H : 「
AAH : ェ
B2H : イ
BAH : コ
83H : Ç
8BH : a
93H : ü
9BH : §
A3H : 」
ABH : ォ
B3H : ウ
BBH : サ
84H : É
8CH : æ
94H : α
9CH : °
A4H : 、
aCH : ャ
B4H : エ
BCH : シ
85H : Ṅ
8DH : ç
95H : β
9DH : ¨
A5H : ・
ADH : ュ
B5H : オ
BDH : ス
86H : Ö
8EH : é
96H : Ø
9EH : º
A6H : ヲ
AEH : ョ
B6H : カ
BEH : セ
87H : Ü
8FH : è
97H : ø
9FH : ¢
27H : ア
2FH : ッ
37H : キ
3FH : ソ


CØH : タ
C8H : ネ
DØH : ミ
D8H : リ
EØH : ▲
E8H : ↑
FØH : Γ
F8H : ε
C1H : チ
C9H : ノ
D1H : ム
D9H : ル
E1H : ▼
E9H : ↓
F1H : Δ
F9H : λ
C2H : ツ
CAH : ハ
D2H : メ
DAH : レ
E2H : 千
EAH : 月
F2H : θ
FAH : π
C3H : テ
CBH : ヒ
D3H : モ
DBH : ロ
E3H : 万
EBH : 日
F3H : Ξ
FBH : σ
C4H : ト
CCH : フ
D4H : ヤ
DCH : ワ
E4H : 円
ECH : ll
F4H : Σ
FCH : ü
C5H : ナ
CDH : ヘ
D5H : ユ
DDH : ン
E5H : 〒
EDH : lll
F5H : Φ
FDH :
C6H : ニ
CEH : ホ
D6H : ヨ
DEH : ゛
E6H : →
EEH : ≣
FEH : Ψ
FEH :
C7H : ヌ
CFH : マ
D7H : ラ
DFH : °
E7H : ←
EFH : ≡
F7H : Ω
FFH : ■

## APPLICATION CIRCUITS

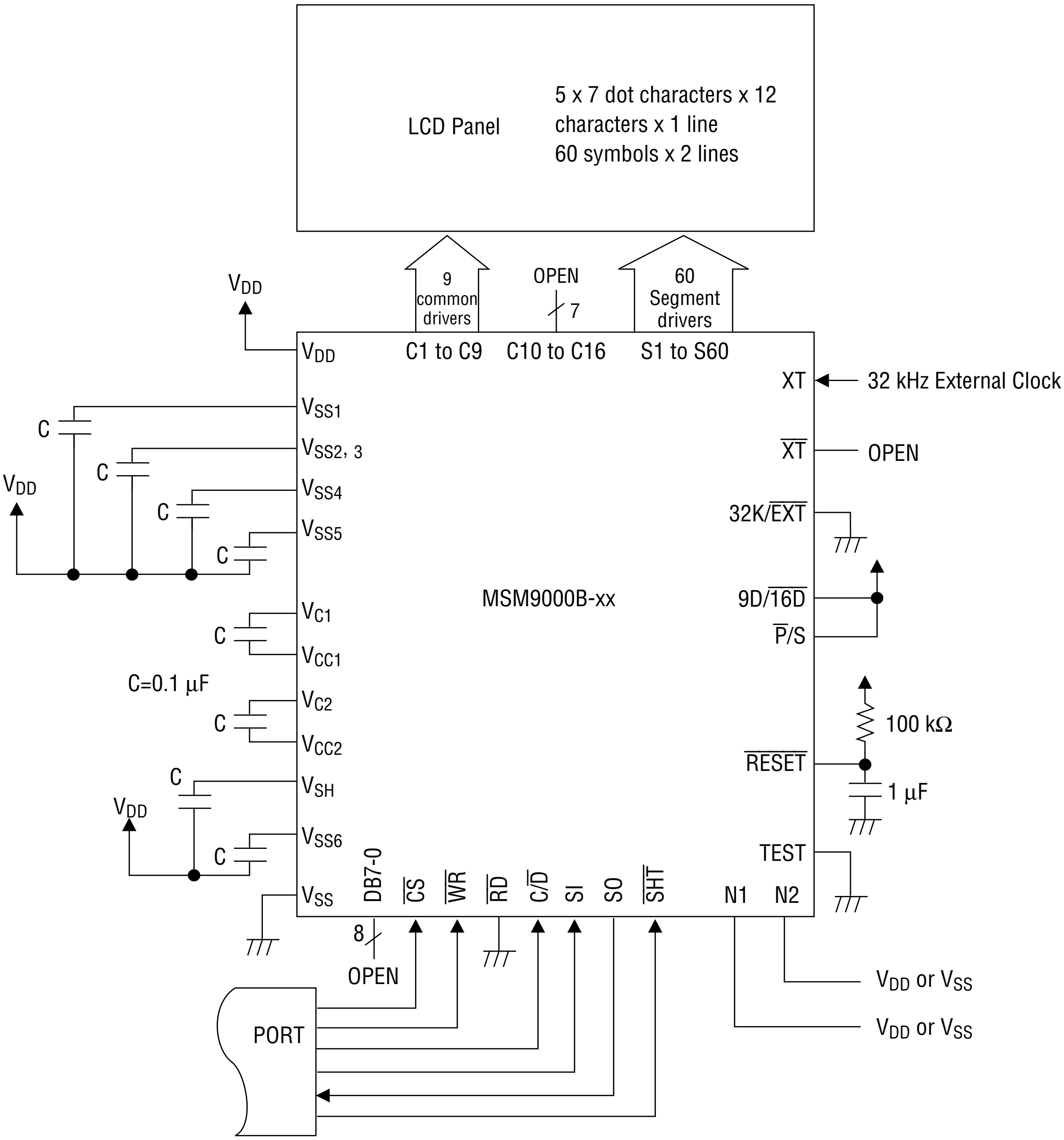
### Example 1

[1/16 duty, parallel interface, crystal oscillation circuit and bias voltage generator used]



**Example 2**

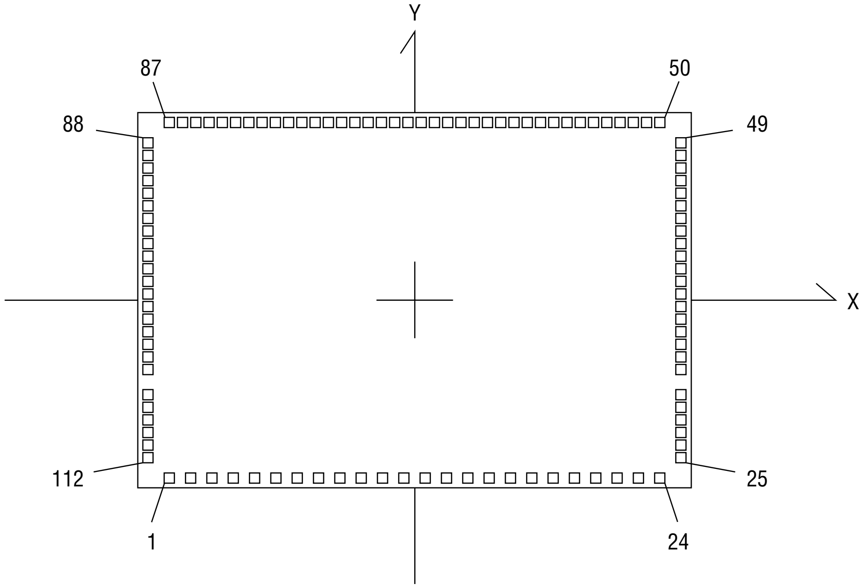
[1/9 duty, serial interface, 32kHz external clock input and bias voltage generator used]



# PAD CONFIGURATION

## Pad Layout

Chip size: 4.76 × 3.29 mm
Bump size: 78 × 100 μm




## Pad Coordinates

| Pad No. | Pad Name | X (μm) | Y (μm) | Pad No. | Pad Name | X (μm) | Y (μm) |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | –2012 | –1508 | 21 | $V_{CC1}$ | 1487 | –1508 |
| 2 | $\overline{CS}$ | –1837 | –1508 | 22 | $V_{C1}$ | 1662 | –1508 |
| 3 | $C/\overline{D}$ | –1662 | –1508 | 23 | $V_{SH}$ | 1837 | –1508 |
| 4 | $\overline{RD}$ | –1487 | –1508 | 24 | $V_{SS6}$ | 2012 | –1508 |
| 5 | $\overline{WR}$ | –1312 | –1508 | 25 | $V_{CC2}$ | 2194 | –1375 |
| 6 | SI | –1137 | –1508 | 26 | $V_{C2}$ | 2194 | –1255 |
| 7 | $\overline{SHT}$ | –962 | –1508 | 27 | $V_{SS1}$ | 2194 | –1135 |
| 8 | SO | –787 | –1508 | 28 | $V_{SS2,3}$ | 2194 | –1015 |
| 9 | DB7 | –612 | –1508 | 29 | $V_{SS4}$ | 2194 | –895 |
| 10 | DB6 | –437 | –1508 | 30 | $V_{SS5}$ | 2194 | –775 |
| 11 | DB5 | –262 | –1508 | 31 | COM9 | 2194 | –605 |
| 12 | DB4 | –88 | –1508 | 32 | COM10 | 2194 | –495 |
| 13 | DB3 | 88 | –1508 | 33 | COM11 | 2194 | –385 |
| 14 | DB2 | 262 | –1508 | 34 | COM12 | 2194 | –275 |
| 15 | DB1 | 437 | –1508 | 35 | COM13 | 2194 | –165 |
| 16 | DB0 | 612 | –1508 | 36 | COM14 | 2194 | –55 |
| 17 | $V_{DD}$ | 787 | –1508 | 37 | COM15 | 2194 | 55 |
| 18 | TEST | 962 | –1508 | 38 | COM16 | 2194 | 165 |
| 19 | N1 | 1137 | –1508 | 39 | SEG60 | 2194 | 275 |
| 20 | N2 | 1312 | –1508 | 40 | SEG59 | 2194 | 385 |

| Pad No. | Pad Name | X (µm) | Y (µm) | Pad No. | Pad Name | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|
| 41 | SEG58 | 2194 | 495 | 81 | SEG18 | –1337 | 1508 |
| 42 | SEG57 | 2194 | 605 | 82 | SEG17 | –1444 | 1508 |
| 43 | SEG56 | 2194 | 715 | 83 | SEG16 | –1552 | 1508 |
| 44 | SEG55 | 2194 | 825 | 84 | SEG15 | –1659 | 1508 |
| 45 | SEG54 | 2194 | 935 | 85 | SEG14 | –1765 | 1508 |
| 46 | SEG53 | 2194 | 1045 | 86 | SEG13 | –1872 | 1508 |
| 47 | SEG52 | 2194 | 1155 | 87 | SEG12 | –1980 | 1508 |
| 48 | SEG51 | 2194 | 1265 | 88 | SEG11 | –2194 | 1375 |
| 49 | SEG50 | 2194 | 1375 | 89 | SEG10 | –2194 | 1265 |
| 50 | SEG49 | 1980 | 1508 | 90 | SEG9 | –2194 | 1155 |
| 51 | SEG48 | 1872 | 1508 | 91 | SEG8 | –2194 | 1045 |
| 52 | SEG47 | 1765 | 1508 | 92 | SEG7 | –2194 | 935 |
| 53 | SEG46 | 1659 | 1508 | 93 | SEG6 | –2194 | 825 |
| 54 | SEG45 | 1552 | 1508 | 94 | SEG5 | –2194 | 715 |
| 55 | SEG44 | 1444 | 1508 | 95 | SEG4 | –2194 | 605 |
| 56 | SEG43 | 1337 | 1508 | 96 | SEG3 | –2194 | 495 |
| 57 | SEG42 | 1231 | 1508 | 97 | SEG2 | –2194 | 385 |
| 58 | SEG41 | 1123 | 1508 | 98 | SEG1 | –2194 | 275 |
| 59 | SEG40 | 1016 | 1508 | 99 | COM8 | –2194 | 165 |
| 60 | SEG39 | 910 | 1508 | 100 | COM7 | –2194 | 55 |
| 61 | SEG38 | 803 | 1508 | 101 | COM6 | –2194 | –55 |
| 62 | SEG37 | 695 | 1508 | 102 | COM5 | –2194 | –165 |
| 63 | SEG36 | 588 | 1508 | 103 | COM4 | –2194 | –275 |
| 64 | SEG35 | 482 | 1508 | 104 | COM3 | –2194 | –385 |
| 65 | SEG34 | 374 | 1508 | 105 | COM2 | –2194 | –495 |
| 66 | SEG33 | 267 | 1508 | 106 | COM1 | –2194 | –605 |
| 67 | SEG32 | 161 | 1508 | 107 | $\overline{\text{RESET}}$ | –2194 | –775 |
| 68 | SEG31 | 54 | 1508 | 108 | 32K/$\overline{\text{EXT}}$ | –2194 | –895 |
| 69 | SEG30 | 54 | 1508 | 109 | 9D/$\overline{\text{16D}}$ | –2194 | –1015 |
| 70 | SEG29 | –161 | 1508 | 110 | $\overline{\text{P}}$/S | –2194 | –1135 |
| 71 | SEG28 | –267 | 1508 | 111 | $\overline{\text{XT}}$ | –2194 | –1255 |
| 72 | SEG27 | –374 | 1508 | 112 | XT | –2194 | –1375 |
| 73 | SEG26 | –482 | 1508 | | | | |
| 74 | SEG25 | –588 | 1508 | | | | |
| 75 | SEG24 | –695 | 1508 | | | | |
| 76 | SEG23 | –803 | 1508 | | | | |
| 77 | SEG22 | –910 | 1508 | | | | |
| 78 | SEG21 | –1016 | 1508 | | | | |
| 79 | SEG20 | –1123 | 1508 | | | | |
| 80 | SEG19 | –1231 | 1508 | | | | |